Integrated processing for microelectronics science and technology

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This paper is a review of integrated processing—an approach to microelectronics fabrication in which sequential processes are linked by wafer transfer through a clean, controlled environment (e.g., high vacuum or inert gas). The approach is rapidly becoming the state of the art in microelectronics research, development, and manufacturing. In microelectronics research, it provides a means for advancing mechanistic understanding and material quality through *in situ* fabrication of test structures and extensive *in situ* diagnostics. In microelectronics development and manufacturing, it promises process simplification, improved contamination control and yield, and potentially more flexible equipment utilization. With increasing emphasis on ultraclean processing, involving control of reactive impurities as well as particles, and on real-time process monitoring and control, applications of integrated processing are moving toward a common ground in which state-of-the-art research techniques can be used to address key issues in development and manufacturing, and provide in return substantive guidelines for manufacturing design and practice.

Introduction

The rapid advances in microelectronics and other advanced technologies have become key factors in the world's economy, and now play a profound role in our lives through both the products and competition they generate. Progress in microelectronics is gated by both science and technology. Ever-changing device, circuit, and system concepts must be quickly and precisely reflected in salable and profitable hardware, thereby requiring new levels of scientific understanding, process control, and manufacturing efficiency.

The strain on manufacturing, development, and research capabilities to keep pace with "runaway" innovation in technology and design is now enormous. Competitive position depends on component reliability levels in the parts per million (allowable defects) and on manufacturing yield levels that were believed unachievable several years ago—levels that must be maintained (and improved upon) in spite of the fact that both the device structures and the processes by which the devices are fabricated routinely challenge our ability to understand and control the essential physical and chemical mechanisms underlying the technology.

The primary driver for chip technology is dynamic random access memory (DRAM). As a measure of the technology challenge, it is noteworthy that the number of discrete process steps in the manufacture of an advanced

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DRAM chip is expected to exceed 500 by 1994. Given the complexity of the processes and the equipment ("tools") used to carry them out, even the "simple" transfer of product between process steps presents a significant danger of creating defects which can ruin a product. There is therefore on the part of process and tool designers a growing effort to either 1) combine sequential process steps within a common (and more versatile) process chamber or 2) physically link two or more process chambers so as to greatly increase the degree of control which can be exercised over all aspects of the transfer of the unit being processed (hence reducing the propensity for defects).

This combining and linking is the essence of what is commonly referred to as *integrated processing*, an approach in which sequential process steps are carried out in advanced processing equipment. Often this consists of multiple vacuum processing chambers linked by a central wafer-transport system; these multichamber tools are also commonly referred to as "cluster tools," insofar as they accomplish a sequence (or cluster) of processes. Alternatively, individual processing tools may be linked by wafer transfer through enclosed environments ("mini-environments") to provide similar advantages in control of the environment experienced by the unit being processed (the "product"). In both cases, the dominant motivation for integrated processing is to achieve substantially greater control over the results of a sequence of processes, which represents a major benefit for associated research, development, and manufacturing aspects.

It is important to distinguish integrated processing, a strategy for linking or combining process tools, from the term *process integration*; this has been used for some time to describe the task of selecting and arranging individual process operations to ensure their compatibility and success in the fabrication of the product, essentially independent of tool details and the means of product transfer between processes.

Integrated processing provides substantial benefit across the spectrum from research to development and to manufacturing.

- For *manufacturing*, integrated processing has so far been most strikingly embodied in the dominance of multichamber, vacuum-based "cluster" processing tools now available from commercial vendors. These typically incorporate several processing chambers and a load-lock (or wafer-introduction chamber), linked by a central robotic wafer handler which moves wafers between the chambers. The industry has moved in this direction because of anticipated advantages in terms of contamination control, reproducibility of process sequences, and possible tooling flexibility. While most tools now available are directed at single-wafer processing in which processing and handling are both at low pressure, a broader range of integrated processing approaches can be envisioned.
- For *development*, the controlled ambient experienced by the wafer during transfer between processes has offered two additional advantages. Because oxidation and contamination can be substantially reduced even in comparison to state-of-the-art clean-room ambients, truly clean surfaces and interfaces can be exploited for process integration, and new device and structure concepts may be realizable for the first time. In addition, reduced contamination between process steps may obviate the need for extra steps—e.g., inspection, cleaning—which are required in current technology.
- For *research*, the ability to control surfaces and interfaces between process steps has proven to be crucial to exploring new structures. At the same time, for research focused on materials and processing science, integrated processing offers several key rewards. First, clean wafer transfer between process chambers and *in situ* analytical equipment permits the use of powerful approaches (e.g., surface analysis) to reveal chemical and physical mechanisms underlying the processes for thin-film and interface fabrication. Second, by combining several sequential processes in a controlled environment which preserves surface and interface properties between steps, simple multilayer structures can be fabricated whose electrical (or other) properties can be directly correlated to process parameters and thin-film/interface characteristics. Third, substantially higher levels of cleanliness and control are expected to enable more sophisticated tailoring of thin-film structures, such as introducing specific concentration gradients through the structure; with control approaching the atomic level, this opens the door to *nanoprocess engineering* of structures, in which the focus is on the detailed atomic-scale properties of the resulting structure as a whole.

In this paper we review some key aspects of integrated processing, focusing on applications which occur in silicon technology and science, although the lessons of this discussion would also apply, e.g., to the packaging, storage, display, and compound semiconductor device technologies. First we provide a more meaningful definition of integrated processing and its relation to ultraclean processing. Then we turn to applications for manufacturing and development, including discussions of associated motivations, tools, process sequences, and crucial issues. This is followed by a discussion of research applications of integrated and ultraclean processing, with particular focus on surface cleaning, low-temperature epitaxy, and thermal oxidation processing for MOSFET structures. Finally we consider the issues of real-time

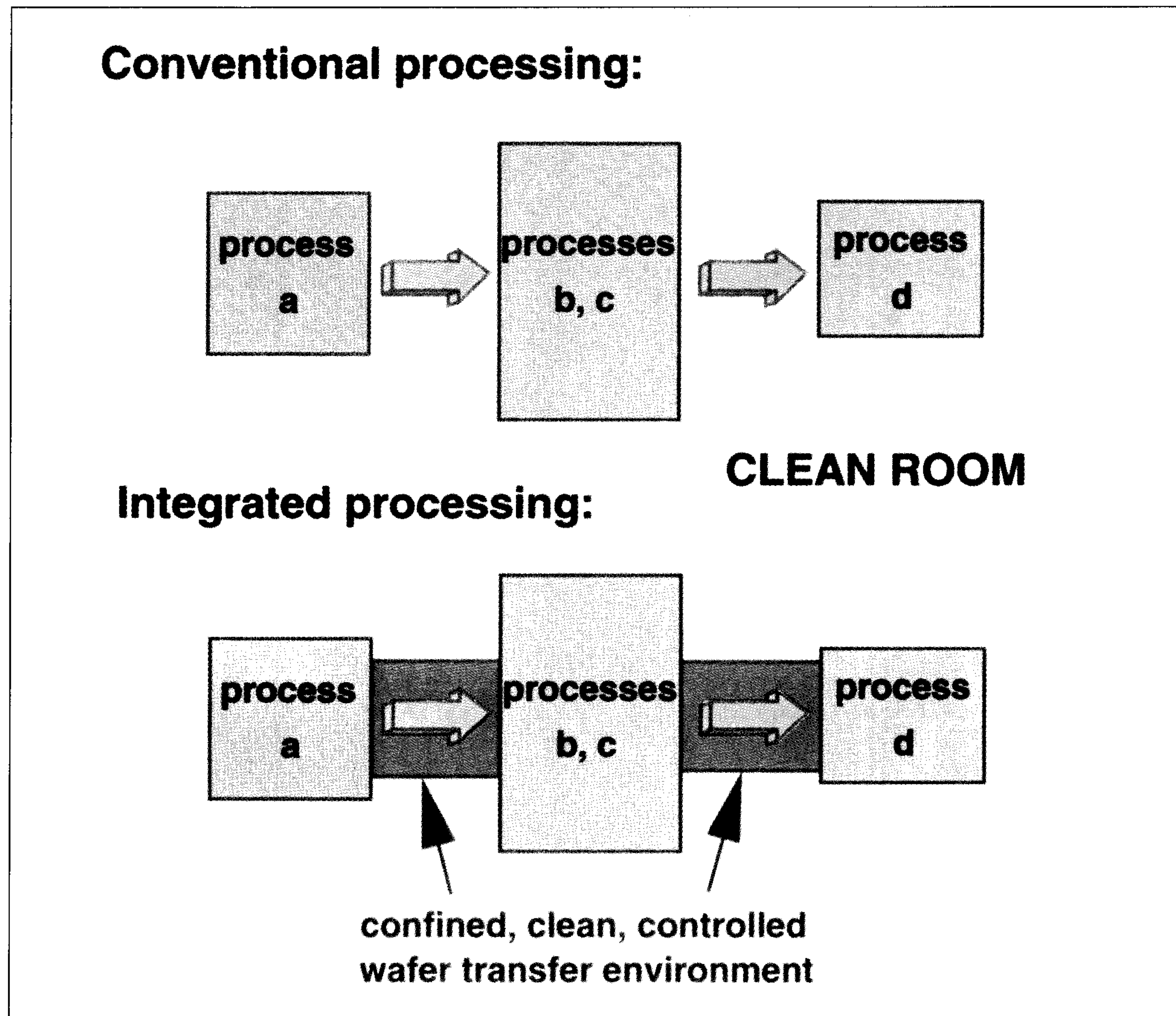


Figure 1

Schematic definition of integrated processing. While conventional processing involves wafer transfer through clean-room ambient between stand-alone process tools, integrated processing imposes a confined, clean, controlled ambient between tools for wafer transfer.

process monitoring and control. A glossary is included at the end of the paper.

Integrated processing

We start with the following definition of integrated processing: *a close coupling between sequential process steps and tools to maintain a wafer in a confined, clean, and highly controlled ambient between process steps, thereby achieving significant advances in associated performance, yield, or cost measures.*

This definition immediately provides a major motivation for integrated processing—contamination control. This advantage is depicted schematically in **Figure 1**, which compares conventional and integrated processing. In conventional processing, separate processing tools which carry out processes such as **a** and **c** are stand-alone systems on the manufacturing floor, and wafers having completed one process in the corresponding tool are transported through the clean-room ambient to the next process/tool; this transfer exposes the wafers to contaminants which include particles, oxygen, water, hydrocarbons, etc. In contrast, if the tools are mechanically linked by a sealed wafer-transfer environment as depicted in Figure 1 for integrated processing, contamination levels during transfer may be notably below those in the clean-room environment. The

integrated process sequence then includes processes **a**, **b**, **c**, and **d**.

- *Scope of integrated processing*

The above definition encompasses several important versions of integrated processing, all of which achieve its major goals, at least in part.

Integrated vacuum processing (IVP) tools

Since many semiconductor processes are carried out at low pressures (e.g., plasma processes, physical vapor deposition, low-pressure chemical vapor deposition) and thus require vacuum pumping, it is natural to structure integrated processing systems around a vacuum chamber which functions as a central wafer handler (CWH) capable of delivering the wafer to any of several vacuum process chambers (process modules) attached to it through isolation (gate) valves, as represented schematically in **Figure 2**. Such systems, often referred to as vacuum cluster tools, have been adopted by a variety of process tool manufacturers and have gained rather broad acceptance in semiconductor manufacturing. They represent an integrated processing strategy predicated on vacuum-based wafer transfer and usually low-pressure processes. While process modules are typically single-wafer, notable efforts have recently been directed toward accommodating types of batch processes as well.

Besides the essential process modules and CWH, they normally include load-lock chambers for introducing wafers from the clean room into the tool as well; additional capability is often included for wafer storage, prebake/cooldown, and alignment. If moving parts which accomplish motion in the CWH do not generate excessive particulates and reasonable vacuum conditions are established, lower contamination levels of both particles and reactive impurities can be achieved. Finally, enhanced cleanliness can be achieved by coupling the vacuum load-lock to environmentally isolated atmospheric-pressure load modules and portable wafer carriers used as mini-environments (see Figure 2 and the discussion below).

Mini-environments

If wafer transfer is carried out though enclosed vessels which are well filtered to remove particles, particulate contamination can be reduced (cf. the clean-room ambient) without resorting to vacuum transfer. This approach, denoted as a "mini-environment" and represented in **Figure 3**, offers potential advantages in capital cost as well as compatibility with atmospheric-pressure-based processes (e.g., thermal oxidation, wet chemical cleaning, lithographic resist processing). In a sense, the mini-environment is an advanced, local, people-free clean room.

A second dimension of mini-environment applications is the choice of ambient. If air is used, oxygen and moisture will be present but can presumably be controlled more accurately than in a state-of-the-art clean room. Alternatively, oxygen-free, dry, or fully inert ambients (e.g., Ar, N_2) may be chosen to minimize reactive impurities as well as particles. Purification and monitoring techniques are available for impurity concentrations in the ppm or ppb level; depending on the impurities which are important, this may be an effective competitor with integrated vacuum processing for reactive impurity control, especially in view of fluid dynamics effects (e.g., inactive layers at surfaces) which reduce diffusion of impurities to active surfaces. Because of these advances, an inert ambient mini-environment represents an integrated processing strategy well matched to atmospheric-pressure-based processing, and typically at lower cost than IVPs.

Portable wafer-carrier mini-environment

An IVP or mini-environment integrated processing system can become a large, rather inflexible apparatus, given that several process chambers and a transfer system between them are permanently coupled mechanically. An alternative which maintains the advantages of integrated processing is to transfer wafers via a clean, controlled storage chamber which is itself portable. The portable storage chamber, as indicated also in Figure 3, can be maintained either as a portable wafer mini-environment (e.g., a SMIF enclosure*) or as a "vacuum suitcase." In either case, when very high cleanliness is desired, the purity level depends on details of the attachment/detachment strategy used to couple the storage chamber to the process chambers.

Multiprocessing (integrated processing in a single chamber)

As indicated by the combinations **b** and **c** in Figure 1, there exist some cases for which several sequential process steps are readily accomplished in the same process chamber, e.g., multilayer metal evaporation or *in situ* doped low-temperature epitaxy. While such situations in themselves do not dictate process tooling which resembles that described above, this application does fit within the definition of integrated processing used here. The necessity to use separate chambers for sequential processes is often determined by subtle aspects of the process tool (e.g., wall impurity adsorption and outgassing) and desired chemistries.

- *Key partners for integrated processing*

Integrated processing thus encompasses several approaches for clean, controlled ambient for wafer transport between processes, thereby circumventing the costs and limitations of ever more difficult clean-room

*Standard Mechanical InterFace (SMIF), a wafer-transfer approach developed by Hewlett-Packard.

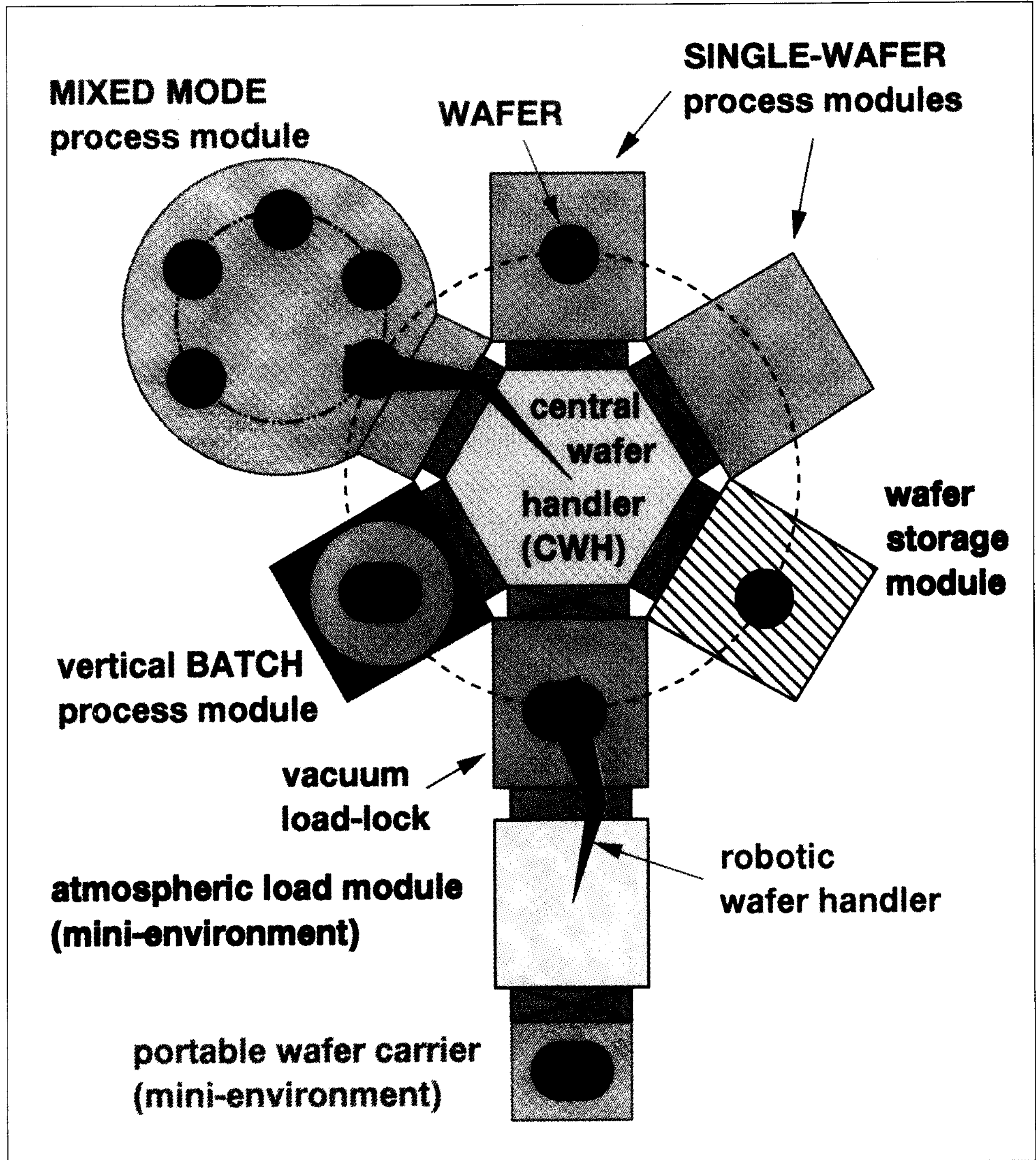
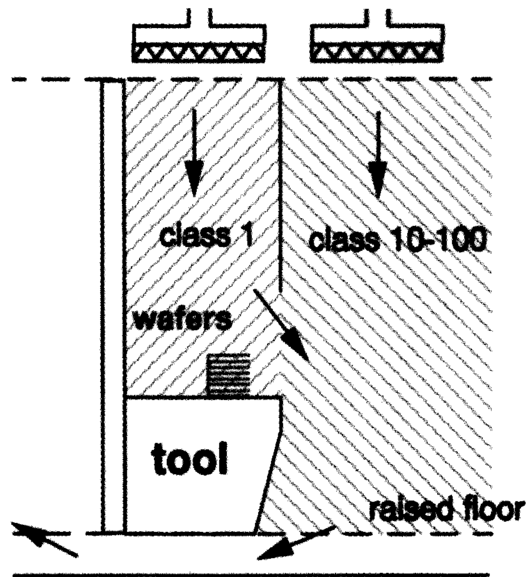


Figure 2

Integrated vacuum processing (IVP) tool. A vacuum-based central wafer handler (CWH) transfers wafers between individual process chambers to achieve an integrated processing strategy which is particularly compatible with low-pressure-based processing.

technology. In some sense, however, integrated processing in these terms is too limited an approach for future manufacturing. It has been widely recognized that particle contamination is increasingly limited by the process tools



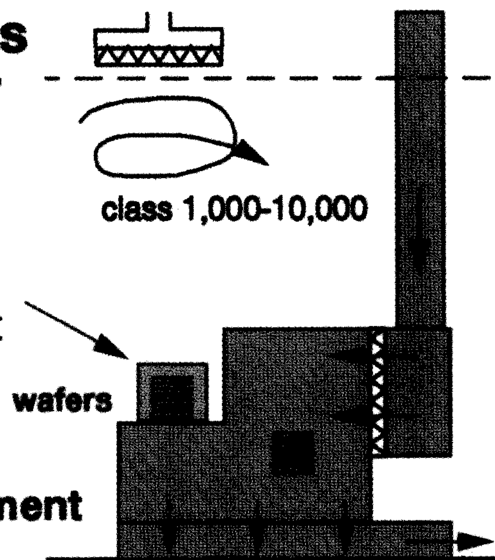


Figure 3

Mini-environment for atmospheric-pressure-based integrated processing. Multiple processes or tools can be combined in a people-free, purified ambient environment at atmospheric pressure to achieve an integrated processing strategy consistent with atmospheric-pressure-based processing or lower cost than IVPs.

and the intrinsic chemistry/physics of the process (which can generate particles directly). Given the investment and technology necessary to develop integrated processing systems, it is a highly desirable and natural step to extend

the scope of integrated processing to a more aggressive goal which would include two other components: ultraclean processing and real-time process monitoring and control.

The inclusion of *ultraclean processing* opens the door to optimizing the gains of integrated processing itself, e.g., reducing reactive impurities as well as particles in order to achieve oxide-free interfaces for radically new structures. That becomes a major goal in the process chamber as well as in the wafer-transfer vehicle, and ultraclean processing becomes a broad and generic theme. In the same way, monitoring cleanliness and the quality of the wafer provides motivation for *real-time process monitoring and control*, in which deviations from intended process and/or contamination level are sensed and exploited to correct and optimize individual processes and also integrated process sequences. Together, these three elements define a fundamentally different generation of process tooling and manufacturability, with the potential for profound advances in process and tool cleanliness, control, flexibility, and reliability, with attendant improvement in product performance and cost.

Ultraclean processing

The cleanliness and control exercised in microelectronics processing technology determine key quality factors such as electrical performance, process yield, and reliability, as depicted schematically in **Figure 4**. Extensive efforts have traditionally been directed toward reducing particulate contamination on wafers by improving clean-room technology. Recently a broader interpretation of relevant contamination has been emphasized, including also 1) particles generated within process tools (by mechanical motions, gas-phase chemical processes, etc.) and 2) reactive impurities present in process tools and in wafer-transfer media.

With decreasing feature sizes and increasing density, lower contamination levels are required to generate acceptable manufacturing yield. It is crucial to understand the contamination-sensitivity of key processes in order to choose a sensible, cost-effective operation point for manufacturing. As shown by the manufacturing process window depicted by the solid curve in Figure 4, this should involve sufficiently low contamination levels to achieve most of the quality benefit which is practical. If contamination levels are too high, variations in process or tool parameters or cleanliness will degrade quality substantially from time to time, as if "falling off the cliff" in Figure 4. This not only reduces yield but often generates a crisis in manufacturing: Because measurements of product quality are often well downstream from the deleterious process step, many wafers may be lost before the problem is discovered, and numerous wafer runs and considerable time may be required to diagnose and correct the failing process step. In contrast, if tools are built for

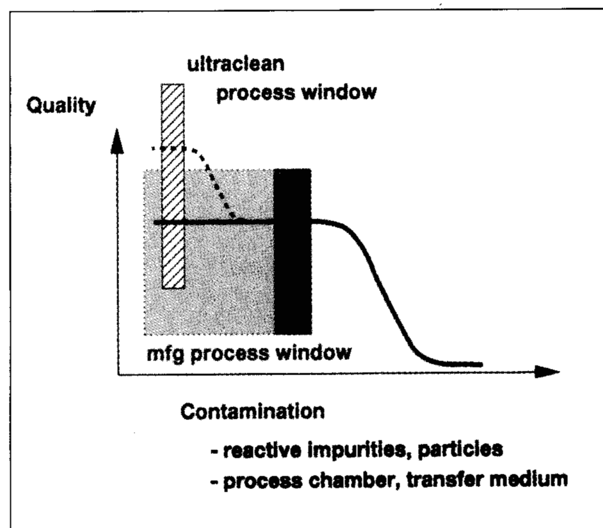


Figure 4

Dependence of quality on contamination level. Quality (i.e., figures of merit such as electrical performance, reliability, etc.) depends on both reactive impurities and particulates, in individual process chambers and in the wafer-transfer environment. Effective manufacturing requires knowledge of the contamination-dependence of quality in order to define efficient process windows and to identify major breakthroughs in quality which may be achievable using ultraclean processing.

much cleaner conditions than are needed, manufacturing costs will not be competitive. These considerations apply to both reactive impurities and particulates, in individual process chambers and wafer transport or load-lock chambers.

It is also important to identify any major enhancements in quality which may be obtained from operation at *significantly* lower levels of contamination, i.e., by ultraclean processing. This domain is indicated by the dashed curve and the ultraclean process window in Figure 4. Recent research (described below) has revealed several cases in which ultraclean processing enables new processes and structures (low-temperature epitaxy being the most notable example) or permits significant improvements in process/properties through identification and control of impurities which are detrimental (or in some cases beneficial).

- *Cleanliness regimes*

Regimes of cleanliness control are shown schematically in **Figure 5**. To reach class 0.1–1.0 for particulates in air ambient, integrated processing mini-environments are a very attractive extension of clean-room technology. By maintaining atmospheric-pressure inert-gas mini-environments, reactive impurity concentrations in the ppb–ppm range can be achieved, and the inactive layer present in viscous gas flow near surfaces will further

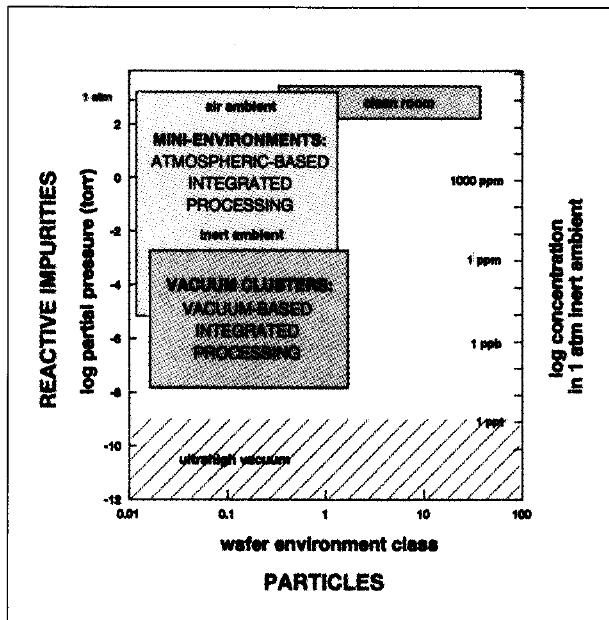


Figure 5

Reactive impurity and particulate reduction through integrated processing. Cleanliness can be achieved through two modes of integrated processing: 1) enclosed mini-environments operating at atmospheric pressure already offer lower particulate levels. By operating these in purified inert ambients, substantial reduction of reactive impurities can also be attained. 2) Vacuum-based integrated processing environments offer reduction of reactive impurities to levels approaching the cleanliness of ultrahigh-vacuum techniques.

suppress the effective impurity contamination rates on wafer surfaces.

When reduced-pressure ambients are employed, as in integrated vacuum processing, levels of reactive impurities can easily be reduced even further. Base pressures of reactor and transfer chambers can readily approach ultrahigh vacuum conditions, and similar low partial pressures of reactive impurities may be maintained in the presence of reactant gas species necessary for processes; thus, equivalent impurity levels (e.g., 10^{-8} torr partial pressure), when related to atmospheric pressure (760 torr), move well into the parts-per-billion (ppb) range.

• *Particulate control*

Particles have long been a gating factor for manufacturing yields as device feature sizes have decreased. Particle densities typically increase sharply with smaller particle sizes, and smaller devices are susceptible to degradation by ever-smaller particles. Thus, the technical challenge and cost of particulate control grow very rapidly with the evolution of the microelectronics technology to smaller feature size and larger chip size.

Major efforts in clean-room technology have reduced particulate contamination through advanced filtration devices, vertical laminar flow, better building and clothing materials, and air showers (i.e., load-locks through which people enter the clean room with a minimum of particulate accompaniment). Class 1 clean rooms (i.e., <1 particle/ft^3 with diameter ≥ 0.5 μm) are becoming common requirements for manufacturing. Integrated processing tools are regarded as promising substantial improvement in particulate minimization and control at reasonable cost.

With improvements in clean-room technology, increasing attention is focused on reducing particulate contamination in processes arising from several sources. First, particles may be present in the chemicals used for the process, whether liquids, gases, or even solids; this underscores the importance of low-particulate chemicals and delivery and monitoring systems which can maintain low particulate concentrations at the point of use. Second, particles may be generated or released by the process tool [1, 2], e.g., through mechanical motion, pumping/venting [3, 4] operations, or flaking within the tool [5]. Third, particles may be formed by the intrinsic process chemistry or physics, e.g., by gas-phase nucleation, as in CVD processes [6, 7] or by a variety of mechanisms in plasma processes [8–11]. Effective control of these mechanisms requires a sophisticated level of understanding, diagnostics, and experimental and theoretical simulation, all of which constitute important areas of current research.

• *Reactive impurity control*

The potential impact of research in ultraclean processing is considerably larger for issues involving reactive impurities, because these influence material and interface quality at essentially *all* sites on the wafer (i.e., $\sim 10^{15}$/cm^2). Thus, materials and processing research can play a major role in elucidating the shape of the cleanliness curve for reactive impurities and thereby help to determine a cost-effective manufacturing point. At the same time, by exploring the ultraclean limit it may be possible to identify major enhancements of quality which are accessible if levels of reactive impurities are substantially reduced (dashed curve in Figure 4). An outstanding example of such an advance is the success of ultrahigh-vacuum chemical vapor deposition (UHV/CVD), which has produced a quantum leap in the quality of low-temperature epitaxial growth (~450–750°C) by sufficient reduction in the partial pressure of oxygen present in the CVD reactor. Ultraclean processing thus offers an outstanding opportunity for process research which is relevant in both the reactor environment (for better processes) and the wafer-transfer environment (for better interfaces).

Ultrahigh-vacuum-based ultraclean systems

Ultrahigh vacuum (UHV) technology provides a reference point for reactive impurity control in ultraclean, integrated

processing. UHV materials, flanges, valves, pumps (turbo-, ion-, and cryo-pumps), and gauging systems represent a well-developed commercial commodity market. With moderate system bakeout (~180°C for several hours) and/or load-locking, the range of UHV ($p_{total} < 10^{-9}$ torr) is readily accessible. Commercial integrated processing systems for manufacturing can be expected to approach the UHV, to perhaps ~10^{-8} torr base pressure with UHV component technology and minimal (if any) bakeout. As seen in **Figure 6**, this provides a low impingement rate for unwanted contaminants: Even at unity sticking/reaction coefficient, 10^{-8} torr pressure corresponds to only ~10^{-2} monolayers of contaminant per second. Finally, note that an appreciable portion of this total pressure typically consists of relatively unreactive species (CO, CO_2, with low reactive sticking probability s) and H_2 (often a harmless, displaceable passivant), while oxygen and hydrocarbon partial pressures are much lower. With appropriate use of load-locks and moderate system bakeout, reactive H_2O can be substantially reduced. By employing UHV-based process reactors, it is possible to achieve much lower reactive impurity contamination than with conventional process technology, providing new possibilities for material and structure quality.

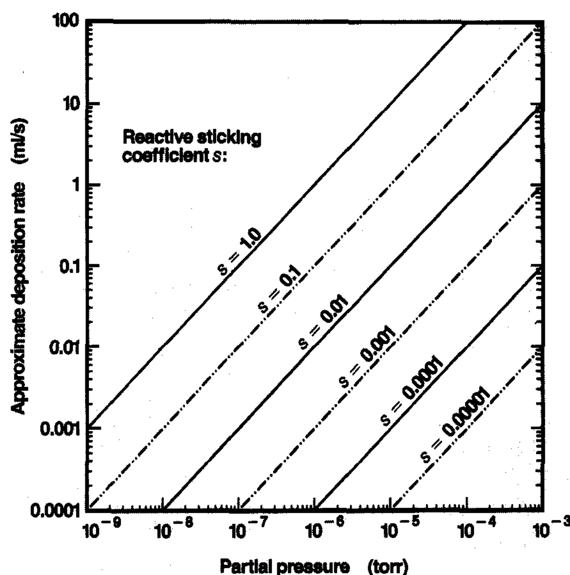


Figure 6

Approximate deposition rate vs. partial pressure. Partial pressures of reactive impurities lead to reaction with wafer surfaces at rates which depend on the reactive sticking probability s.

Inert-ambient atmospheric-pressure-based systems
UHV-based ambients also provide a target for reactive impurity control in atmospheric-pressure, inert-ambient mini-environments, but the situation is decidedly more complex. While atmospheric pressure ambient may cause greater desorption of species from walls, it also effectively suppresses total reactive impurity adsorption over a fixed time due to the presence of an inactive layer for fluid flow near solid surfaces.

Besides the wafer transport environment, cleanliness of the process environment remains an important determinant of process quality. In all cases, the purity of reactants for chemical processes and the interaction of reactants, products, and impurities with chamber walls can substantially alter material on the wafer. These complexities are greater at higher pressures in the viscous/fluid flow regime (cf. molecular flow at lower pressures), so that atmospheric-pressure processes may be a more difficult case to understand (if not to control) than vacuum-based processes.

Ultraclean reactant sources, purification, and delivery
With regard to reactive impurities, ultraclean processing conditions are important not only for the goal of preventing wafer surface degradation by unwanted impurities from the process or wafer-transfer ambient, but also from the chemicals and gases utilized as reactant sources for growth or etching processes. The most crucial hurdle to be overcome is the purity required in the inert gas: As seen in Figure 5, matching the reactive impurity concentration of a 10^{-8} UHV ambient requires cleanliness of the inert gas in the system of ~10 ppt (parts per trillion), or 10^{-11}. Pioneering work has been carried out by T. Ohmi and coworkers at Tohoku University to develop techniques for reagent purification, delivery, and characterization, as well as to evaluate the consequences of ultrapure reagents for process and material quality. Examples include reagent and ambient purity levels required of different processes and tool approaches [12]; exploitation of UHV-compatible materials with special methods for stainless steel surface passivation [13–16] and tube welding [17]; ultraclean components for gas-delivery systems [12]; the engineering and monitoring of reactant delivery systems with continuous flow for purity [18–20]; the purification of water to reduce dissolved oxygen and thereby suppress surface oxidation [21, 22]; the use of atmospheric-pressure ionization mass spectroscopy (APIMS) to investigate drying of wet chemicals and related impurity concentrations [23]; and the properties of HF solutions [24, 25], the role of surfactants [26], and the use of ultrapure anhydrous HF [27]. Some of these results have made an impact on manufacturing strategies by providing enabling technology elements (e.g., fabrication methods for gas-delivery systems), by supplying specific

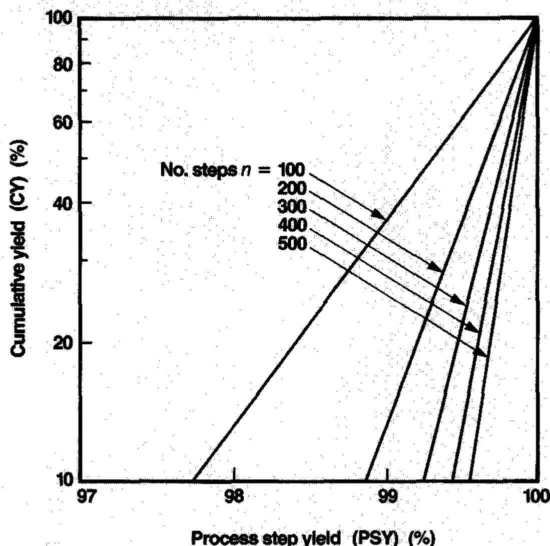


Figure 7

Manufacturing yield. Total manufacturing yield decreases rapidly with the yield for each process step as the number of process steps becomes large.

technical details, and certainly by heightening awareness that impurity control relates directly to manufacturability and yield. Tools for monitoring gas purity levels in the ppt–ppb range under atmospheric pressure ambients are commercially available.

Manufacturing applications

• *Manufacturing yield as a driving force*

Process yields and product performance and reliability are critical to manufacturability. With the mushrooming number of process operations in semiconductor processing, the sheer numbers, even exclusive of the degree of difficulty, make it highly probable that one of the many steps needed for product fabrication will compromise the product, even though processes may meet specifications more than 99.8% of the time (where the cumulative process functions within $\pm 4.5\sigma$ of the performance nominal value).

Figure 7 shows the expected yields for sequences of various lengths vs. yield for each process step (in the number of standard deviations to either side of the mean). With well-controlled steps, a sequence of 200 steps at 99.8% yield per step generates yield losses of 23% (cumulative yield 77%) from (nonparticulate) defects randomly occurring during the process steps. A 500-step process would lose 52% of its yield with similarly performing individual processes. To achieve the same 77% yield as for the 200-step case, each of the steps in the 500-step case would have to be improved to a 99.95% level.

Intense competition in manufacturing quality and cost, together with much more complex processes, has raised the requirement for future manufacturing yields. In 1995, a DRAM production sequence with more than 500 process steps will have to show cumulative yields above 90% for the full sequence in order to manufacture competitively. To meet this challenge, each process step will have to operate within its specification limits no less than 99.98% of the time. Given the assumption that 130 chips are printed on a single wafer, any given process (tool) would be allowed to cause a "killer" defect on a single chip only once every 36 wafer passes. To put this into perspective, each process step in a 77% yielding process today is allowed to "kill" a similarly sized chip once every six wafers. The reduction factor indicated over the next four to five years for process "faults" is then approximately $6\times$. Note that these calculations include only parametric losses associated with process variations; they do not consider area-dependent mechanisms such as might be caused by extrinsic contamination. The latter will serve to further degrade yields by probably $4\times$ because of increasing chip size and scaling to smaller feature sizes in both vertical and lateral dimensions.

If the overall process yield target is raised to >95% (an increasingly common goal), the defect contribution rate for a process would again have to be cut by >50%, to one for every 75 wafers run through that process sequence. These levels of performance will require profound efforts toward defect elimination. Approaches will have to include

1. Eliminating process steps through better process, device, and circuit design.
2. Improving process integration strategies to reduce the number of process steps.
3. Eliminating measurements and inspections which add no value to the product.
4. Designing processes and devices for manufacturability, thereby making them more forgiving of process variations.
5. Improving process and tool control.
6. Reducing process development and tool development cycle times to accelerate development and yield learning.

Typical process and tool development cycles have included most of these activities. In the future, however, a well-managed product development effort will have to go much further, and in a much shorter time, toward optimizing and balancing the interactions between the efforts suggested above. Integrated processing activity begins with item 3 in the list above and includes the entire remainder of the list, peaking with item 6.

• *Integrated processing (cluster) tools for manufacturing*
Thus far, physical integration of process steps has most often been accomplished by grouping two or more process chambers around a central wafer handler. Several types of such integrated processing or cluster tools are available from a number of equipment manufacturers. They generally introduce product wafers from the clean room to the central wafer handler (CWH) by means of an antechamber, or load lock, which is controlled for ambient and pressure. The CWH then passes the wafer to and between the process chambers according to programmed routings, and finally returns it to a holding station in the load lock.

Properly designed, cluster tools offer several advantages in process control and defect reduction. One is standardization of the path, time, and exposure to contaminants during wafer transfers between processes. A second is a reduction of the number of times that a wafer must be "handled" in moving between operations. A third is the general reduction of the exposure of the wafer to potentially contaminating atmospheres (including even the best clean room); that is a key driver toward cluster tools and represents a substantial part of the tool design effort.

Today's cluster tools serve process sequences carried out at high vacuum (e.g., physical vapor deposition), low vacuum (dry etching, plasma-enhanced CVD, and thermal CVD), and atmospheric pressure (photolithographic processing and thermal oxidation of Si). They typically address a single wafer at a time in the CWH but can process up to five wafers simultaneously (the number of process chambers physically clustered around the CWH).

To accomplish crucial process sequences in a cluster tool environment, commercial tools now combine thermal and plasma-enhanced CVD in a cluster along with sputtering and reactive ion etching (RIE) modules. Such combinations enable the tailoring of a CVD film to cover topographical steps and fill high-aspect-ratio trenches through a series of deposition and etchback steps. Capability for "soft" sputter-clean of the wafer surface to remove contaminants (e.g., native oxide) is also being built into cluster tools. Finally, clusters are now being designed and considered which will perform the traditional hot-process steps, including annealing, oxidation, and CVD. The newest designs promise to combine atmospheric- and low-pressure and high- and low-temperature steps around a single CWH. As represented in Figure 2, they may handle either single wafers or batches of wafers, depending on the economies of the individual process operations.

• *Spectrum of processes and conditions*
Integrated processing is certainly destined to struggle with the often difficult problems of process compatibility, particularly because optimization of cluster tool design and architecture depends on the mix of processes for which the process modules are suited. As seen in **Figure 8**, today's semiconductor manufacturing processes span a very large spectrum of temperatures (−100°C to nearly 1200°C) and pressures (10^{-7} torr to atmospheric pressure). With the broad variety of physical mechanisms and chemical recipes involved, it seems clear that the most useful cluster tools will be designed to accommodate process diversity. For example, integrated processing of the FET/CMOS gate dielectric stack requires 1) wet surface cleaning (room temperature, atmospheric), 2) thermal oxidation (high temperature, atmospheric), and 3) LPCVD polysilicon deposition (moderate temperature, low pressure). In spite of the interest in all single-wafer processing, all three of these processes are now carried out as batch processes and may compete as such with their single-wafer rapid thermal counterparts. And the emergence of mixed-mode process modules (Figure 2) may provide a version of batch processing even for those processes (e.g., plasma-based) where single-wafer processing has been a long-expected trend due to larger wafer sizes.

• *Integrated processing evolution*

Historical perspective
Early integrated processing dealt with somewhat easier situations in which the sequential processes were quite similar in character—i.e., in chemistry, temperature, and pressure. Wafer cleaning is such an example, wherein "dip tanks" were lined up in rows to facilitate handling and prevent operator mistakes. Later, cleaning operations were automated through the application of robots to move cassettes between the tanks and with the advent of spray tools, which accomplished all of the wet operations in a single chamber, i.e., by multiprocessing.

More recently, photolithography sequences, with temperatures sometimes ranging from near freezing to >400°C have been linked in clusters which include apply, bake, chill, and develop modules, all at atmospheric pressure (or slightly below). Novel balancing techniques for air pressure and flow within the enveloping mini-environment prevent cross-contamination by restricting heat and chemicals to only those sections of the cluster where they are needed. Integrated photolithography clusters have provided three important benefits—substantial improvements in overall process control (yield), higher throughput, and increased utilization of the very expensive exposure tools which are the heart of the photo operation.

In the past several years, multilayer metal sputter deposition at low pressures has been a prominent focus for vacuum cluster tools, using several sputter-deposition modules attached to a CWH. Multiprocessing has also been employed for multilayer deposition within a single process chamber. The need for multilayer metallization

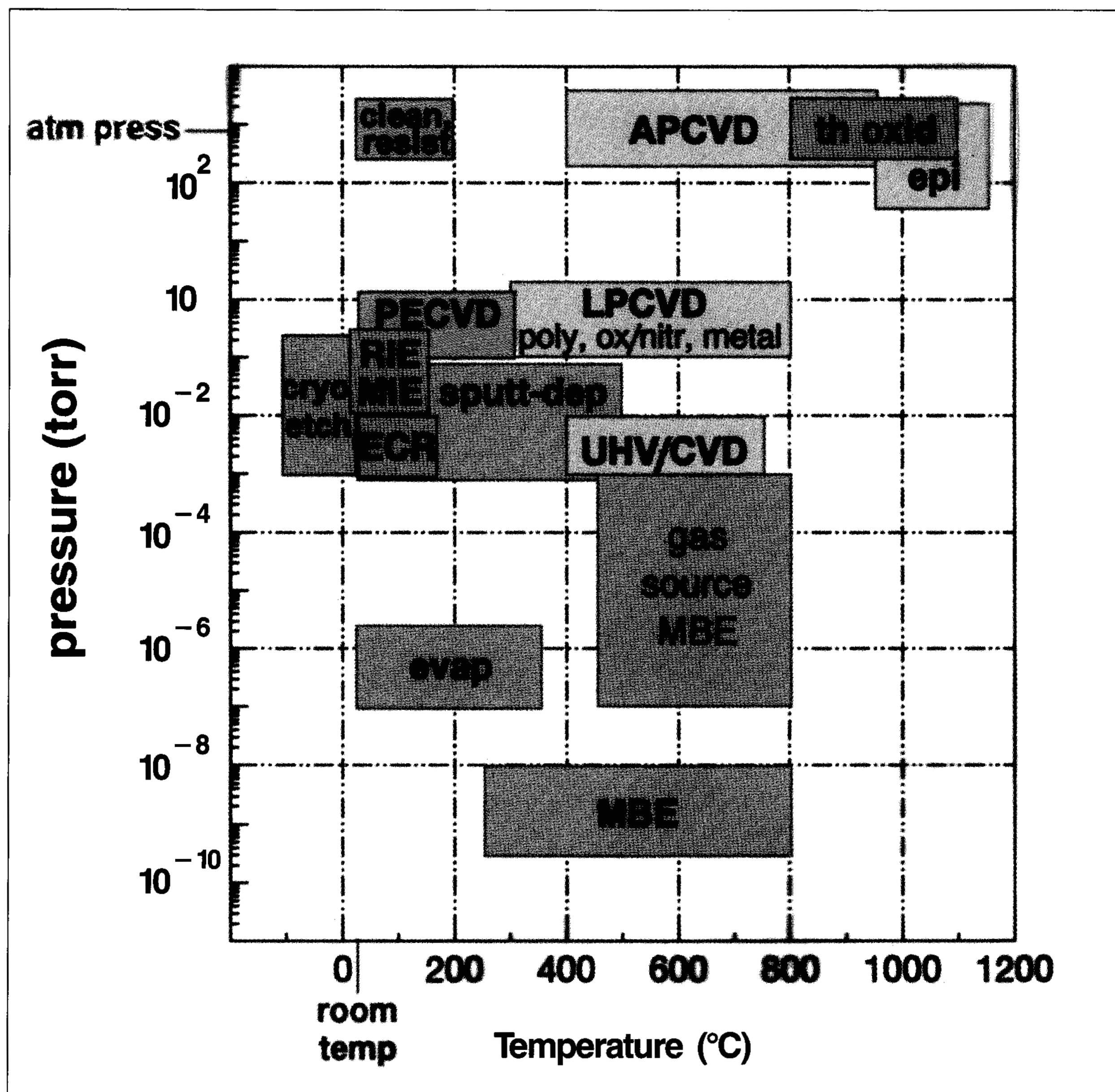


Figure 8

Semiconductor processes as a function of pressure and temperature. Although all of the processes can be carried out as single-wafer processes, many can also be accomplished as batch (multiwafer) processes.

and the similarity of pressure/temperature conditions across a variety of sputter-deposition processes has made this an important and early entry for integrated processing to manufacturing. A similar trend toward integrated processing has been apparent for reactive ion etching modules, where cross-contamination could be a more difficult issue; however, the environmental control offered by integrated processing already provides a profound process advantage.

General trends

In some respects, then, the easier versions of integrated processing and tool clustering have already been exercised. Two factors are now driving integrated processing toward a broader spectrum of applications in which sequential processes vary widely within the integrated process sequence. First, the development community benefits from exploiting the advantages of integrated processing through the possibility it offers of mixing and matching process

combinations that will result in the highest-quality materials and structures. The attendant cleanliness of process chambers and wafer-transfer ambients provides substantial improvement in both film and interface quality because of the reduction in particle contamination and reactive impurities (H_2O, O_2, etc.). Second, the manufacturing tool community can take advantage of the opportunity to optimize throughput and cycle time with the greater variety of available equipment approaches (e.g., single-wafer vs. batch).

The application of integrated processing in semiconductor microelectronics presents a total change in approach from stand-alone tools and processes in a clean room. Successful implementation of integrated processing is probably best achieved in a gradual, evolutionary transition, since 1) much learning will be encountered and required along the way, and 2) the high cost of process tooling in any case makes it highly unlikely that a next-generation factory can be dominated by integrated processing, because of economic constraints alone. The focus, then, is on those specific process sequences ("key clusters") which are amenable to integrated processing and at the same time offer profound opportunities for higher quality, higher yield, lower cycle time, and, hopefully, cost-effectiveness.

Most clustering activities are intended to reduce product costs by increasing yield sufficiently to more than repay the costs of more sophisticated and advanced integrated processing tools (although in some cases the clustering may be intended to realize new materials and/or structures—and attendant performance—which are not achievable in any other way). Yield enhancement is expected principally from reduced contamination, reduced wafer handling, process simplification, and reduced need for inspections.

Physical vapor deposition (PVD) clusters

Process sequences for interconnect (and certain other features) typically involve sputter-deposition of interlayer films for adhesion and diffusion barrier functionality, followed by deposition of the interconnection metallization. There is substantial current interest in incorporating into this sequence a "soft" (low-ion-energy) sputter "preclean" (pre-cleaning) of the wafer surface. For advanced integrated processes, sputter-deposition requires high levels of cleanliness in the CWH, since fresh metal surfaces are very reactive. Integrated process tools even for strictly physical vapor deposition already raise important issues of cleanliness and cross-contamination between chambers.

Efforts are also directed at extending PVD clusters to include LPCVD metallization, RIE etching steps, and annealing (involving temperatures ranging from room temperature to perhaps 700°C) and in some cases to atmospheric processes. The presence of reactive gas species in CVD and RIE (cf. inert gas in sputtering) represents a potential source of contamination for the CWH and sputter-deposition chamber as the wafer is removed after these processes. Rapid thermal annealing would best be accomplished under vacuum for pressure-compatibility with the CWH.

Reactive ion etching (RIE) clusters

RIE clusters constitute a major portion of existing integrated processing tools and applications. Key process sequences motivate the inclusion of PECVD, LPCVD, and RTA modules to integrate deposition, etching, and annealing processes. While the process pressures are fairly comparable, the differences in process temperatures and reactant gases in these clusters are large, and chemical contamination and cross-contamination issues become more of a concern.

The combination of LPCVD and RIE/PECVD is an especially important cluster for two kinds of applications. First, deposition followed by RIE ("dep/etch") can be used to obtain planarized deposited thick films. Second, conformal CVD deposition of insulators over vertical sidewalls of conductor wiring lines, followed by RIE to remove the film from only the horizontal surfaces, can be effectively employed to build insulating "sidewall spacer" structures on the sides of the wiring lines; in this way, no photomasking sequence is needed, and a crucial insulating layer is constructed by a self-aligned process on the sidewall of a conductor within a single cluster.

Hot-process clusters

In the application of integrated processing, there has recently been increasing focus on high-temperature oxidation and LPCVD process steps, commonly called "hot processing," and toward associated wafer precleaning processes. Hot processes involve complex tool structures (e.g., quartz furnace tubes with high-temperature ovens surrounding them), and vacuum pumping in the case of LPCVD. Most hot processes have traditionally been carried out with large batches of wafers (batch processes) in order to accommodate the tool requirements of these processes and to achieve sufficient wafer throughput for inherently slow process chemistries.

Despite the complexity of hot-process tools, vacuum-compatible load-locks and even integrated batch process modules are beginning to appear in order to achieve enhanced cleanliness control of the batch reactor conditions and enable the fabrication of key structures (key clusters). One set of such examples includes insulator/electrode structures, such as in the FET gate dielectric, the DRAM capacitor, and bipolar isolation structures. At the same time, the advent of rapid thermal processing tools, and recently of single-wafer tools for hot

processes, opens another avenue toward integrated processing of hot-process sequences; indeed, it can be expected that single-wafer rapid thermal integrated processes will play a major role in such applications as FET gate and DRAM capacitor clusters in the future.

It will prove challenging to exploit the advantages of integrated processing for these hot-process cluster sequences, particularly within the demands imposed by cost-effective manufacturing. For one thing, it will be critical to integrate the final surface preclean into the cluster, which underscores the importance of developing controlled vapor precleaning processes and tools; this is currently the subject of substantial research. A final wafer preclean before the clustered hot processes may require atmospheric-pressure conditions (or nearly so), temperatures up to perhaps 400°C, and certainly the use of corrosive gases (such as HF) which jeopardize the vacuum and cleanliness integrity of tools in general. The presence of residual contamination from corrosive precleans could severely degrade the quality of process and product in associated thermal oxidation reactors, where O_2 and sometimes H_2O are employed at temperatures up to ~1120°C.

Similar complexity is to be found in the chemistries utilized in LPCVD, since deposition of polysilicon and oxide and nitride insulators play important roles in many key hot-process clusters. These processes operate at low pressures (typically ~1 torr) and moderately high temperatures (~550–800°C) and use extremely hazardous gases both as primary reactant species and as dopants. The potential for these gases to etch metal chamber walls and thereby transport metal contaminants in vapor phase onto insulator films on the wafer is another concern. Finally, it should be noted that development of single-wafer process modules for LPCVD has been rather slow, which may signal the persistence of a batch process approach even in the domain of integrated processing.

Despite the considerable problems to be overcome in the exercise of integrated hot processes and associated precleans, several prototype systems are already available from a number of equipment suppliers. Interest from semiconductor manufacturers is reportedly very strong, having increased substantially over the past year as migration to new device generations highlighted the need for further improvements in process control for thin-insulator structures.

Integrated processing: Vacuum and atmospheric processes

While many processes utilized in semiconductor manufacturing require reduced-pressure operation (as seen in Figure 8), atmospheric-pressure-based processes are essential today and may remain so in the future. Atmospheric-pressure-based processes dominate wafer cleaning, photolithography, thermal oxidation, and conventional epitaxial growth, and they represent virtually the only approach to wafer polishing and other physical manipulations of the wafer. In addition, most in-line measurements of wafer parameters are most reasonably carried out at atmospheric pressure. The importance of atmospheric-pressure-based processes makes it clear that they play a role as important as do vacuum clusters.

Already built to maintain vacuum integrity, vacuum clusters are clearly able to realize significantly lower levels of reactive impurity contaminants. The central wafer handler on a vacuum cluster is its own mini-environment. The transition zone through which wafer cassettes pass between the storage box and the load lock on a vacuum cluster tool has already been discussed as the most ubiquitous form of a mini-environment, which serves, in one form or another, virtually all cluster tools. Such combinations of vacuum-based and atmospheric-based chambers reflect strategies which are emerging to enable ultraclean, integrated processing in future manufacturing.

- *Vacuum cluster tools*

The design and architecture of process modules and integrated vacuum processing systems raise numerous technical issues, which are outlined below.

Load-locking and ambient buffering

It is useful to think of the integrated processing tool as linking three environments—process chamber, central wafer handler, and clean room. The intention of the CWH is to maintain a contaminant-free environment for wafer transfer between process steps, which for IVPs means low total pressures. No matter how high the pumping speed on the CWH, it is extremely difficult to maintain high vacuum (low pressures, $\leq 10^{-6}$ torr) with reasonable wafer throughput if wafers are introduced from the clean room by simply opening a valve directly between the clean room and the CWH, because water vapor from the clean room adsorbs on the CWH walls and desorbs slowly (unless they are held at ≥150–200°C). Thus, high-vacuum conditions in the CWH effectively dictate the use of a load-lock chamber between the clean room and the CWH. Intrinsic mechanisms (see below) which generate or dislodge particles by means of rapid pumpdown further necessitate the use of load-lock chambers.

If process gases adsorb significantly on chamber walls and have a high vapor pressure, they can produce a background of residual gas species in the CWH which represent unwanted reactive impurities there (though they were desired reactants in the process chamber). In extreme cases this may necessitate the use of an intermediate chamber between the process chamber and the CWH.

Venting and pumpdown

For integrated vacuum processing systems, wafers must undergo pumpdown to high vacuum upon entering an IVP

tool and venting upon exit; if some processes are carried out at atmospheric pressure (or under viscous flow conditions at lower pressure), significant pumpdown and venting behavior is also encountered prior to transfer between those process chambers and the CWH.

Pumpdown and venting processes can be significant sources of contamination. While reactive impurities may be fairly straightforward to deal with (through oil-less pumps, purified venting gases, etc.), particle contamination is more difficult. Also, condensation of H_2O (or hydrocarbon) vapor occurs during pumpdown and nucleates on very small particles, causing these to grow heavier and fall on wafer surfaces [4], so that when the H_2O evaporates, the particle has been gettered to precisely the wrong place. Multichamber tools with sufficient cleanliness can reduce H_2O concentrations to negligible levels, but the issue remains at load-lock chambers which are employed for wafer entry or exit from the tool system; there, a dry or inert gas purge prior to pumpdown helps. Even in the absence of condensation phenomena, turbulent flow at higher pressures accompanies fast pumpdown or venting, expelling particles from surfaces. Slow pumpdown and venting cycles are a more reliable way to suppress particle contamination associated with condensation [28] or flaking from the reactor walls. However, since slow pumpdown requires minutes per cycle, it becomes advantageous to do batch pumpdown and venting.

Process pressure regime: Low (vacuum) vs. atmospheric pressure

As indicated in Figure 8, current process technology encompasses both low-pressure and atmospheric-pressure processes (a striking example is the importance of CVD processes in both domains). This mixture appears within key clusters; e.g., the FET gate dielectric stack is normally practiced with atmospheric surface clean and thermal oxidation, followed by low-pressure CVD polysilicon (all in batch mode). This presents a difficult choice for integrated processing strategy: Either a very fundamental process change must be made to achieve compatible pressure regimes through the entire cluster, or the tool architecture must accommodate pumpdown/venting *within the cluster* to handle the pressure discontinuity between processes, e.g., by batch pumpdown/venting as described in the previous section.

Other, more fundamental aspects of the processes also enter the picture. Some processes simply do not provide high-quality materials growth at higher pressure (e.g., because of gas-phase nucleation and consequent particle formation, as in low-temperature CVD growth of SiO_2), while other processes offer higher throughput and even better quality at high pressure because of the different physical mechanisms of reactant and product flow under these conditions.

Dry vs. wet processing

Wet processes are essential portions of overall process technology, particularly in surface cleaning, resist processing, and some areas of etching (e.g., selective etching of unreacted metal vs. silicide in the salicide process). There is a strong driving force toward dry (vapor-phase) processes, primarily for advantages in contamination control (low particulates) and controllability. Significant research along these lines is now taking place (e.g., vapor HF for oxide removal), although advances in liquid purification and monitoring as well as physical phenomena unique to the liquid state (double layer, etc.) may guarantee wet processing a major role for the foreseeable future. By the use of mini-environments coupled to IVPs, one can expect that both wet and dry processes can be accommodated within ultraclean, integrated processing.

Single-wafer vs. batch processing

Single-wafer processing is a strong trend in manufacturing process technology. As cost advantages push wafer size larger (to ≥8-in. diameter), tool dimensions must be scaled up dramatically while maintaining a high degree of process uniformity across the wafer. This is a problem particularly in processes such as plasma deposition, dry etching, sputter deposition, and evaporation, where a geometric volume of space above the wafer surface must be reserved for the intrinsic mechanisms of the process; in these cases, tool size increases rapidly with wafer size for batch processes, and it is desirable to look at single-wafer processing as a trend toward continuous-flow manufacturing. In an era of increased attention to process monitoring and real-time control, single-wafer processing also offers improved diagnostic access, especially in comparison to batch LPCVD, oxidation, or annealing, where 50–100 wafers may be stacked only a short separation apart (~1 mm).

On the other hand, the enhanced throughput of such batch processes has made them very common in manufacturing. The relatively larger fraction of solid surface represented by wafers in a batch reactor provides the possibility of more efficient reactant utilization, as well as a distribution of reactive species seen by the wafer which is less dominated by chamber walls than by identical wafers. Finally, processes which attain very high material quality may require low reaction rates and throughput, thus necessitating other approaches (such as batch processing) to gain economical throughputs.

One could argue that, in general, single-wafer processes [29] offer substantial advantages in the quality and performance of the product, while batch processes provide lower manufacturing cost. Since competitive manufacturing requires attention to both performance and cost, we can

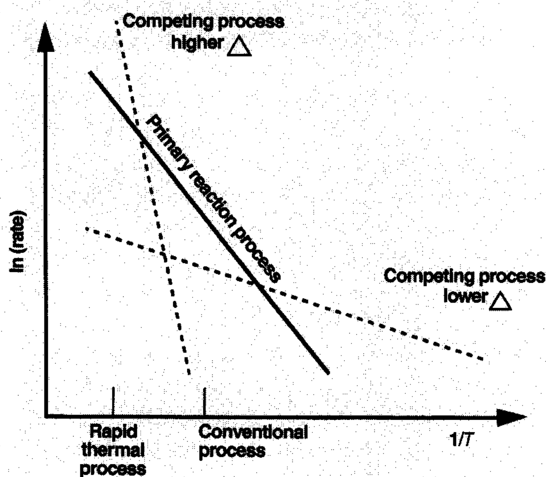


Figure 9

Competing reactions during processing as a function of wafer temperature. For a given primary reaction process, competing processes having a relatively high activation energy Δ become relatively more important at high temperatures, while those having a relatively low Δ become more important at low temperatures.

expect a variety of potential system solutions. Several examples are illustrative:

- By adopting a versatile hardware architecture for integrated process tooling, both batch and single-wafer process modules can be accommodated. This feature has been indicated in Figure 2, in which a vertical batch process module has been incorporated into a cluster tool system, using a vertical cassette load module coupled to a vertical batch reactor above it. An example is the ASM Advance 600 system, in which the CWH operates single-wafer to load vertically oriented wafer cassettes, which then access vertical batch reactors. Multiwafer cassettes are an efficient way to cycle between atmospheric- and low-pressure regimes within the guidelines of slow roughing and venting as needed for minimizing particulate generation, both in the load-lock/introduction of wafers to the cluster tool and from the CWH to any atmospheric-pressure process modules which may be attached (e.g., thermal oxidation).
- By enlarging a single-wafer cluster to accept multiple wafers, higher effective module throughput can be achieved for the same process (i.e., longer process time per wafer is available at the same module throughput). This approach, already introduced by several tool vendors and depicted schematically as the mixed-mode process module in Figure 2, also offers the possibility of enhanced uniformity due to averaging over multiple process sites in the module.
- Rapid thermal processing (RTP) exploits single-wafer processing with rapid lamp heating to achieve short-time processing and enhanced temperature programmability and range. Since chemical reaction rates are thermally activated and therefore usually increase dramatically with temperature, much higher process reaction rates and manufacturing throughput can often be obtained in *chemical* processes using RTP, potentially overcoming a significant drawback to single-wafer processing. At the same time, by using a rather dramatically shorter process time (e.g., a few seconds compared to ≥10 minutes) at higher temperature, the total thermal budget expended in the process may in favorable cases be kept within the constraints of the overall process integration strategy.

Rapid thermal processing

In its use of thermal cycles involving higher temperatures and shorter times, RTP offers both advantages and disadvantages in quality compared to continuous processing in conventional hot-wall furnace-type reactors. First, the short time scale is consistent with single-wafer processing strategy. Second, RTP often provides a notable improvement in process cleanliness. Desorption of impurities or products of wall reactions can be low because of the cold-wall condition. More importantly, since the time during which the wafer is at reaction temperature is short, the total impurity flux which can lead to incorporation at the wafer is minimized; this feature has led to advantages for RTP in such applications as silicide formation anneal (which should be in an oxygen-free environment), even for tools which have not been designed for ultraclean operation.

The use of higher temperatures and shorter times in RTP highlights another important and fundamental issue, namely the role of competing reaction pathways. Given a primary reaction process which is intended to be exploited, there usually exist a number of other reaction pathways which will occur simultaneously and hence compete with the intended reaction; if the competing reactions are deleterious to the material or structure being fabricated, it is essential that the competing reactions proceed much more slowly than the primary reaction *at the reaction temperature employed in the process*, a temperature which is quite different in RTP compared to conventional processes. This situation is indicated schematically in **Figure 9**, which compares the kinetics of a primary reaction process to that for competing reactions with higher and lower thermal activation energies Δ. By carrying out a conventional process in a rapid thermal mode, the relative contribution of competing reactions may be changed, either for the better or worse.

The impact of competing reaction processes may be seen in the example of thermal oxidation processes for growth of the gate dielectric of a MOSFET. Activation energies for thermal oxidation are ~2 eV or below ($\Delta \sim 2$ eV for initial linear growth and ~1 eV for subsequent parabolic growth) [30]. Dopant diffusion in Si involves $\Delta \sim 3.5$–4.0 eV [31], so that redistribution and broadening of any existing dopant profile (already substantial in the range ~700–800°C) will become a greater concern at higher oxidation temperatures, as in rapid thermal oxidation. Although this does not create a problem in conventional approaches to FET fabrication, it may impose important process integration constraints for more advanced device structures and necessitate the use of lower-temperature processes for dielectric growth (e.g., PECVD [32]). Two other competing reactions during thermal oxidation become relatively more important at higher temperatures because of their high activation energies. First, at higher oxidation temperatures (≥950°C), viscoelastic relaxation of the SiO_2 becomes important and relaxes the amorphous network, leading to improvements in stress-related electrical properties of the MOS structure. Second, at very high temperatures, reaction at the Si/SiO_2 interface decomposes SiO_2 (with $\Delta \sim 3.83$ eV [33]), with attendant electrical and physical consequences, including local etching of the Si surface and the formation of defects in MOS structures; these phenomena are most apparent under low oxygen concentrations at high temperatures, but they can certainly be expected to contribute to electrical defect properties even under thermal oxidation conditions.

Reactor wall temperature—hot-wall vs. cold-wall reactors
With the need for better control of reactive impurities in processes and for a wider variety of process choices, the importance of reactor wall temperature is increasing. In hot-wall batch reactors, such as those commonly used for atmospheric-pressure oxidation or low-pressure CVD for polysilicon (polycrystalline silicon) or insulator deposition, a considerable number of wafers are processed in an environment which is isotropic, thermally and often chemically. The long thermal time constants of reactor and wafers in this geometry favor temperature reproducibility and uniformity while impeding the use of more dynamic temperature–time recipes (e.g., RTP). Since the same reactions occur on the walls as on the wafers, the chemical environment can be more uniform; e.g., in the case of reagents such as SiH_4 for Si deposition, where reactive sticking probabilities are low, low depletion and excellent uniformity can be attained [34]. In the general case, however, wall reactions may contribute to depletion and therefore to nonuniformity along the reactor and across the wafer, and reaction products from the walls can become impurity sources for the wafers as well. Clearly, the fundamental surface and gas-phase chemistry of the particular process is a major factor in determining the suitability of a given reactor configuration.

Cold-wall reactors present more difficult challenges for achieving temperature uniformity across the wafer, but they also offer significant advantages. With the temperature insufficient to initiate reactions on the walls, the wall contribution to depletion effects is reduced. Cold-wall systems do not generally generate reaction products which could compete with the intended reactant. With wafer heating carried out by a heated susceptor or external lamps radiating through transparent reactor walls, cold-wall configurations lend themselves readily to single-wafer processing and improved *in situ*, real-time diagnostics techniques for process control. Finally, for processes and sequences which might intentionally exploit wafer temperature changes during the process, their shorter thermal time constants are an advantage.

With more complex chemical systems, "warm-wall" reactors merit increasing attention. For example, liquid or solid organometallic sources such as those used for CVD of metals might normally be used in a cold-wall configuration, but the low volatility of these sources (cf. gases) makes them readily condensible on gas line and reactor walls at room temperature. Therefore, it becomes necessary to heat gas lines and reactor walls sufficiently to desorb condensing reactant without dissociation, creating the need for a reactor wall arrangement intermediate between cold-wall and hot-wall conditions, i.e., a "warm wall."

Multiprocessing (single-chamber integrated processing)
Conventional process tools have already been used to combine successive processing steps within a single tool as indicated in Figure 1, i.e., as an embodiment of multiprocessing. Examples include surface sputter-cleaning combined with sputter-deposition dry etching; integrated thermal oxidation, annealing, and polysilicon deposition in a rapid thermal processing tool [35]; pattern etching of "stacks" of materials, as in multilayer metallization interconnections; and wet immersion or spray cleaning, in which several different solutions of very reactive chemicals are sequentially cycled into the wafer chamber, with each intended to remove a different type of contamination (as opposed to moving wafers between wet chemical tanks with intervening water rinses). In a related context, plasma cleaning of the plasma deposition, sputtering, or etch tool has been utilized to ensure reliability and product reproducibility (e.g., avoiding product degradation due to particulate generation as microflakes from the walls).

The research community has recently extended the range of multiprocessing within the context of single-wafer processes [36]. By using a single-wafer lamp-heated rapid thermal processing system to carry out a sequence of rapid thermal CVD and rapid thermal oxidation steps, each with

different gas conditions (reactant, pressure, etc.), multiple layers have been grown with their thicknesses controlled by the RTP temperature–time profile; this approach, termed "limited reaction processing," has been demonstrated in the fabrication of MOS capacitors [37, 38] and SiGe heterojunction bipolar transistors [39]. *In situ* sequential deposition of stacked oxide/nitride/oxide layers by a similar approach has also been demonstrated [40], and remote plasma-enhanced CVD has also been employed to fabricate MOS structures incorporating multilayer dielectrics [41–43]. Accomplishing key aspects of integrated processing within the framework of multiple process steps in a single reactor has recently been extended to a process reactor incorporating single-wafer thermal, plasma-enhanced, and photo-enhanced processes [44, 45].

The execution of integrated processing via multiprocessing—i.e., multiple processes in a single reactor—is likely to play an important role in future manufacturing by increasing process simplicity and interface control (major motivations for integrated processing in general). However, applications of this approach will depend on crucial issues of process chemistry and compatibility, e.g., as indicated above in the discussion of reactor wall temperature. If the next process step is subject to adverse influence from the chemistry of the previous step and the reactor ambient cannot recover quickly, loading effects in the reactor will rule out the use of multiprocessing for that sequence. On the other hand, experience to date makes multiprocessing a promising approach.

- *Mini-environments*

Mini-environments (atmospheric-pressure-based integrated processing systems) are in some sense the result of two considerations. First, some cluster process sequences (e.g., wet cleaning, resist processing) involve fundamental atmospheric-pressure process conditions, so that the integration of these processes in a cluster tool system is most effectively a mini-environment (indeed, a vacuum cluster tool operated entirely at inert 1 atm ambient could be a suitable, though overly expensive, mini-environment). Second, and probably more pervasive, the mini-environment represents a strategic approach to the factory of the future, in which specific tool clusters are linked by an ultraclean people-free wafer transport and storage system.

In the latter application, wafer-handling and storage operations which were formerly done under filtered air showers in the clean room can be combined with specific process tools within a people-free area which is highly clean with respect to particles and, in more advanced cases, reactive impurities. Single-wafer tools such as the series of apply/bake/chill/develop for photolithography, with their small size and often-repeated sequences, are being clustered into temperature- and humidity-controlled mini-environments around optical stepper tools for lithography. Larger single-wafer tools, such as rapid thermal processors, are more difficult to link physically, as are batch tools for oxidation, annealing, LPCVD, and cleaning, so that a variety of tool cluster design strategies involving mini-environments are under consideration for development.

An ultraclean environment for wafer transport and storage can be implemented in a variety of ways ranging from fully automated, robot-populated ultraclean rooms to nitrogen "tunnels" and even to total wafer handling under vacuum. But these approaches all exact significant prices with regard to technology change, space, capital cost, maintainability, and/or productivity.

Fortunately, there are more moderate alternatives. A number of efforts in the industry have focused on a fab (manufacturing facility for fabrication of micro-electronic devices) architecture which minimizes the volumes of space that must be kept ultraclean, i.e., a minimum-size mini-environment. The concept requires a novel wafer cassette box and a mechanism for transfer of wafers between the cassette box and cluster tools or mini-environments without exposing the wafers to the people-populated clean room. Hewlett-Packard developed the wafer-transfer technology, called Standard Mechanical Interface (commonly referred to as "SMIF"), which is now marketed in the form of "SMIF pods"; these small, portable mini-environments are moved to a tool system, attached, and then opened only to the tool system so that a robotic device can exchange wafers between the SMIF pod and the tool system. The robotic control associated with SMIF and mini-environment operations also provides a built-in wafer inventory and tracking methodology.

A large number of semiconductor manufacturers have successfully experimented with mini-environments and SMIF pods in both new construction and low-cost fab upgrades for improved contamination control. The most impressive examples is the commitment of an entire manufacturing fab (>70 000 ft^2) to mini-environments and SMIFs by the Taiwan Semiconductor Manufacturing Corporation. This fab, which began full production in 1990, provides air at better than class 1 to the mini-environments which serve the fab process tools, while the remainder of the environment in which people work has relaxed garmenting guidelines and is said to operate at roughly class 1000. Taiwan Semiconductor reports that the mini-environments are completely effective in excluding room-generated particles from wafer-handling areas, a claim which has been confirmed by outside engineers and scientists. The savings in operating costs will pay for the slightly higher installation cost for the fab within a year or two.

It is interesting that integrated *vacuum* processing tools are leading the way to the use of mini-environments, i.e.,

atmospheric embodiments of integrated processing. The central wafer handlers in current PVD and RIE clusters are linked to vacuum load-lock chambers, which in turn are connected to small, partially enclosed areas flushed by very clean air; these chambers could be converted rather straightforwardly to true mini-environments fully sealed from the outside ambient. This would be a notable step toward the architecture depicted in Figure 2, consisting of a vacuum cluster tool, an attached mini-environment, and a portable mini-environment (SMIF).

Advanced stepper tools for optical lithography are routinely delivered with clean-air mini-environments with temperature and humidity control. Entire photolithography clusters, including the steppers, have also been outfitted as full temperature- and humidity-controlled mini-environments. Other tools such as vertical furnaces and rapid thermal processors are sold routinely with HEPA- and ULPA-filtered laminar air flow functionality in totally enclosed wafer-handling areas. Even "wet decks" for wafer cleaning, probably the earliest form of integrated processing tools, are now commonly enclosed and served by a robot within a mini-environment.

In today's clean rooms, air-filtration apparatus can account for as much as 35% of the cost of building a fab and for equally significant portions of the operating costs of the facility. The garmenting used to keep people-generated particles away from wafers is, as well, expensive in terms of maintenance, floor space, and personal productivity. The proven performance of mini-environments in attenuating room particle counts by $\geq 10^6\times$ strongly suggests that fab architectures built on a mini-environment strategy are a way to break the spiraling costs associated with ensuring clean air around wafers. All indications are that clean-room areas where people work need be no better than class 1000 (as at the Taiwan Semiconductor facility) if the wafer transport and process functions are contained in mini-environments; garmenting requirements may then be considerably reduced.

One recent estimate put the cost reduction for converting to mini-environments for air handling alone at 50–70% below that needed to upgrade to a class 20 environment (estimated for a small fab, including SMIF hardware). Since the equipment to upgrade to class 20 does not guarantee particle densities *at the wafer surface* under class 1 air showers, adoption of the mini-environment approach appeared a clear choice. Other costs can also be expected to come down in a mini-environment-based fab. With reduced room air flow, raised floors are no longer needed, since the relatively low volume of air required to maintain class 1000 or better can pass under or between tools. Relaxed particulate cleanliness in the people area also reduced costs associated with arranging separation between the wafer-and-people handling area (advanced clean room) and the equipment support area ("core" area, used for pumps, gas supplies, etc.). Factory floor layouts are no longer constrained by air-management concerns. Equipment in the areas where people work can be designed for reliability, performance, and cost-effectiveness, without high concern for cleanliness. And tool maintenance and rearrangement activities need only affect one tool at a time, leaving adjacent tools fully operational. Thus mini-environments are evolving naturally into tool and fab architectures and strategies for both technical and economic reasons.

- *Impacts on fab operation, architecture, and economics*

The implementation of ultraclean, integrated processing through vacuum cluster tools and mini-environments provides a path to simplification of tooling and process integration as well as enhancement of fab flexibility, with major potential cost savings and efficiency gain. Though the path to achieving these advantages is not simple and not guaranteed, they constitute a strong motivation for fundamental changes in process tooling approaches for the future.

Simplification of tooling

With the advent of integrated processing tools, the total number of tools (cluster tools) between which wafers (cassettes) must be carried diminishes. At the same time, efforts toward standardization of wafer-handling interfaces are starting to bear fruit, resulting in similarities between tools with regard to the way they handle wafer or cassette input/output. While there are tens of different RIE, PVD, photolithography, CVD, and cleaning steps, these are being increasingly integrated into a smaller number of different cluster tools. Indeed, one can envision that in an advanced manufacturing line a specific type of process (e.g., RIE) might be executed many times, but always in the same type of process module or cluster tool in various places on the factory floor. Realistic projections for integrated processing and tool clustering indicate that the number of major tools which are fundamentally different will drop to fewer than ten in manufacturing lines in the 1995 time frame.

Given the extraordinary cost of manufacturing tooling, its simplification promises major economic efficiencies. These will be significantly gated by how well the tooling industry moves toward standard protocols for defining how process modules and cluster tools should be linked and exchanged to achieve an open tool architecture. Such standards must include such information as physical specifications for attachment of process and transfer chambers, placement accuracies and ranges for wafer handlers which move wafers from one chamber to another, and software and networking protocols for integrated control systems. With sufficient implementation of standards, integrated processing tooling can consist of

process modules and wafer handlers which can be mixed and matched to customize integrated processing systems for highly competitive applications. The absence of standardization may greatly slow the rate at which the industry deploys integrated processing because of the high risk associated with the choice of a particular cluster tool system, and of course competitiveness will be compromised.

Simplification of process integration
The utilization of ultraclean, integrated processing can also lead to considerable process simplification. With the ability to transfer wafers between processes without contaminating the wafer surface, it is expected that fewer cleaning and inspection steps will be needed; for example, oxides grow readily on metals or on Si upon exposure to room air and must then be cleaned before the contact metallization is deposited, either by wet chemical processes and rapid transfer of the wafer into the deposition tool, or by *in situ* sputter-cleaning in the tool. With a much more highly controlled wafer environment through critical process sequences, fewer inspections should be required.

With these advantages from integrated processing, new kinds of thin-film structures and properties can be fabricated for the first time. At the same time, to exploit ultraclean, integrated processing for more effective fabrication of known structures may require better mechanistic understanding of processes. Examples of both are discussed below in the section on research applications.

Fab flexibility
As integrated processing serves to reduce the number of different tools on the production floor, it also increases the overall flexibility of the fab. Where a tool set once was application-specific, clustering should facilitate modifications and upgrades to the "condensed" tool set of the future in order to quickly implement strategic new processes and process sequences. Such modifications could be as simple as transferring a process from an identical process module in development, purchasing and installing another type of process module (rather than an entire tool system), or making simple hardware changes to the existing process module (new gases, etc.).

With greater tooling flexibility, manufacturing costs should be reduced. The fab may be able to manufacture a broader range of product types with the addition of only a few specialty modules or tools. Conversion of the manufacturing line to the next technology generation may involve the replacement of only some of the process modules, not the entire tool set, while the clean-room air-handling systems and most of the wafer handlers should need no modification or replacement. Of perhaps the greatest importance, future fabs populated with clusters of similar tools may be better able to mutually support one another: Demand "bubbles" in one product line may be met, without loss of revenue, by quick, low-cost conversions of comparatively few tools in other fabs which are less heavily utilized.

Research applications

- *Process understanding and control as a motivation*

Materials and processing research depends substantially on new levels of characterization and control of the process environment to obtain fundamental mechanistic insight and to develop new levels of process control and material/structure quality. Detailed study of the wafer surface and the process environment can be carried out before, after, and in some cases even during the process, using a variety of sophisticated techniques from surface science as well as mass and optical spectroscopies. At the same time, the use of ultrahigh-vacuum-based process environments and ultrapure reactants provides an opportunity to minimize the presence of unwanted chemical species and enables studies which clearly address fundamental chemical and physical mechanisms.

With these motivations toward ultraclean processing conditions and advanced *in situ* diagnostics, the use of integrated processing in research applications becomes essential for several reasons. First, and most important, process learning and improvement can be considered relevant only if it improves electrical properties or some other important figure of merit. Electrical (or other) test structures for these properties require several sequential processes for their fabrication. Since the cleanliness control exercised in research on specific processes would not be exploited if wafer transfer between these processes were not equally clean, relating figures of merit to process parameters and properties requires the linking of multiple process chambers by ultraclean wafer transfer vehicles, i.e., integrated processing. Second, elements of integrated processing (specifically, ultraclean wafer transport between chambers) are essential for using advanced techniques of surface analysis: Because the vacuum conditions typical for most processes (Figure 8) are incompatible with the UHV conditions needed for surface-analytical methods, wafers must be transferred between process and surface-analysis chambers under ultraclean conditions. Third, some exploratory device structures require multiple processes to be carried out in different process chambers without air/contaminant exposure between processes.

- *Integrated processing systems for research*

The largest number of research systems which use integrated processing are those devoted to multichamber molecular beam epitaxy (MBE) [46, 47], where physical

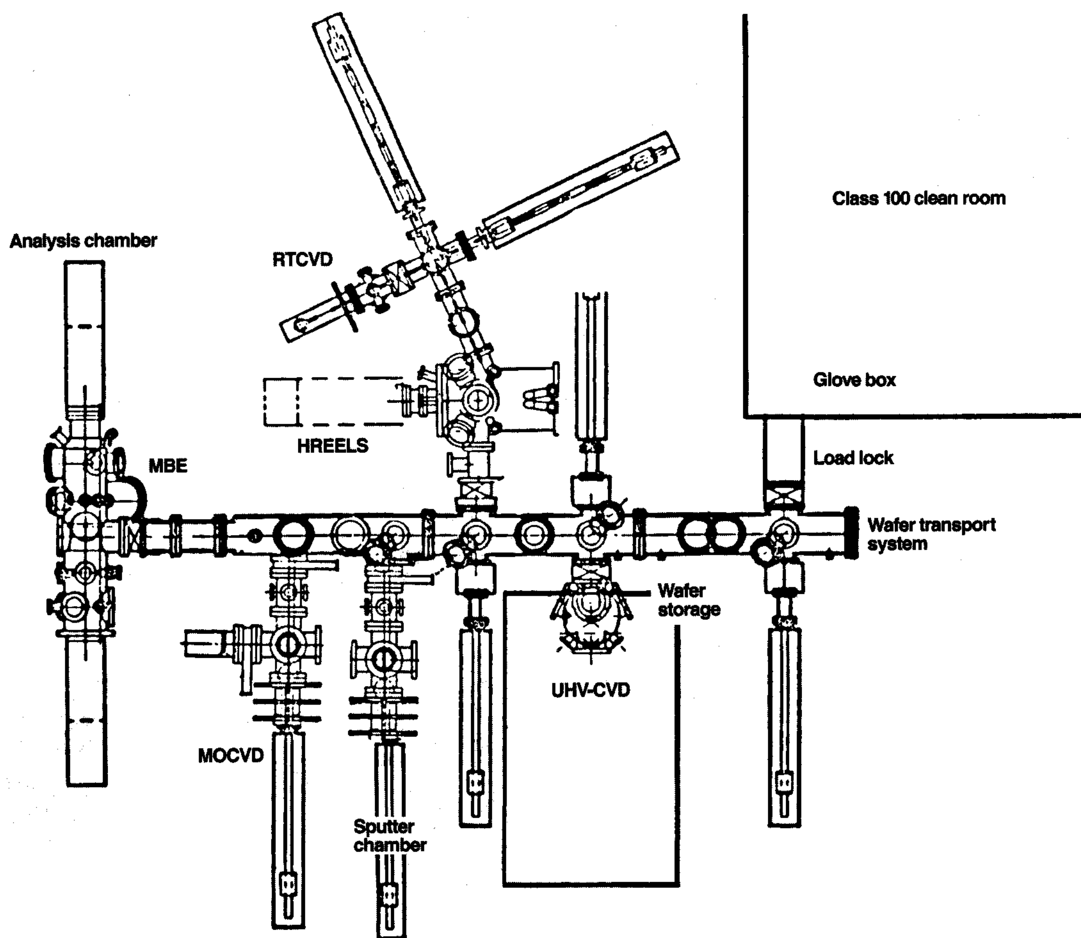


Figure 10

Example of ultraclean, integrated processing system for research into thermal processes (top view). Multiple process chambers and *in situ* analytical techniques are combined into an all-UHV environment. From [51], reproduced with permission.

vapor deposition is carried out under UHV conditions to produce epitaxial homostructures and heterostructures. Because of the low-pressure regime in which MBE operates (Figure 8), surface-analytical methods are directly compatible with MBE processes. This growth technique also offers the profound advantage that deposition can be controlled on essentially an atomic scale to build semiconductor layer structures as desired, permitting fairly straightforward fabrication of a variety of exploratory device structures and early learning about their properties and potential.

For a broader range of *chemical* processes (plasma-enhanced CVD, thermal CVD, etc.), the situation becomes considerably more complex because most, if not all, process environments are fundamentally *incompatible* with surface analysis from the viewpoint of the partial pressure of reactive species (Figure 8). However, the expected benefits of integrated processing for research goals have motivated the construction and utilization of advanced, UHV-based multichamber integrated processing systems for single-wafer remote plasma-enhanced CVD [48, 49] and for thermal [50, 51] processes.

An example [51] of an advanced research system utilizing integrated processing is shown in **Figure 10**. This custom all-UHV system incorporates multiple reactor chambers for (primarily) thermal processes as well as a variety of *in situ* diagnostic techniques. Wafers having a 3.25-in. diameter are routinely utilized, with wafers transported and sometimes used in four-wafer batches. The process reactors include 1) a quartz hot-wall vertical

furnace reactor for low-pressure processes (low-temperature UHV/CVD epitaxy, polysilicon or insulator CVD), atmospheric-pressure thermal oxidation and annealing of a four-wafer batch; 2) a quartz, single-wafer rapid thermal processing reactor for low-pressure CVD, atmospheric-pressure oxidation, or annealing, all under rapid-thermal, nominally cold-wall process conditions; 3) a stainless-steel, single-wafer CVD system for metallo-organic CVD processes (e.g., metal CVD); 4) a sputter chamber for ion-beam cleaning/conditioning of the surface using a broad-beam source; 5) multiple MBE deposition sources to deposit metal contacts through a shadow mask (or blanket films, e.g., for CVD nucleation studies on clean metal surfaces). In addition, a small clean room (class 100) houses a load-locked glove-box system maintained under purified N_2 ambient for wafer loading and precleaning operations; precleans include wet HF dip, UV/O_3 treatment, and vapor HF, with mass spectrometric sampling capability for observing volatile products during the process.

This system also provides for extensive *in situ* diagnostics, including studies of surface chemical bonding and composition by X-ray (XPS) and uv (UPS) photoemission spectroscopies, Auger electron spectroscopy (AES), ion-scattering spectroscopy (ISS), high-resolution electron energy loss spectroscopy (HREELS) for vibrational studies, secondary ion (SIMS) and neutral (SNMS) mass spectroscopy, and depth profiling; surface structure by low-energy electron diffraction (LEED) observations and spot-profile analysis; surface morphology by scanning electron (SEM) and scanning Auger (SAM) microscopy at modest lateral resolution (~1–2 μm); gas-phase analysis using mass spectroscopy for ambient species; and thermal desorption mass spectroscopy (TDS) for volatile surface species.

Such a system clearly offers major advantages for processing research. Final cleaning steps can be executed within the inert ambient, then followed by a variety of thermal processes, all in an ultraclean, integrated processing environment. Such integrated process sequences can readily include some key integrated processing sequences, such as MOSFET gate oxide processing, which is discussed in detail later. In addition, the surface conditions before and after specific processes can be assessed by using *in situ* analytical techniques. Taken together, these capabilities represent not only a path to advanced understanding and control of key processes and sequences, but an opportunity to prototype and develop guidelines for successful integrated processing in manufacturing.

• *Surface cleaning and passivation*

Surface cleaning processes play a pivotal role in integrated processing. Well-controlled, reproducible cleaning procedures are essential if process studies are to be sufficiently well defined to realize the advantages of ultraclean, integrated processing. And precleaning processes themselves are the focus of substantial process research as well as integral parts of key cluster sequences, e.g., cleaning for epitaxial growth or contact metallization.

Although wet cleaning sequences involving oxidants, reductants, and etchants are ubiquitous and effective in today's manufacturing technology, there is growing interest in their replacement by vapor-phase cleaning processes where possible because of their controllability (as dry processes), reduced particulate levels (cf. liquids), and compatibility with integrated vacuum processing systems. Some vapor-phase processes are well known, but others are needed to effect a major impact on wafer-cleaning strategies. For example, Si beam cleaning is effective in removing oxides from Si or Ge through MBE [52–54] or CVD [55] Si or Ge deposition to form volatile SiO (or GeO) products, but it requires high temperatures (~750–900°C) which are incompatible with the preservation of advanced semiconductor structures (e.g., sharp boron doping profiles). Thus, new low-temperature vapor-phase processes are needed, especially those which can effectively clean patterned wafers (e.g., to remove oxide from Si or metal in the presence of nitride or photoresist masks).

Both liquid and vapor (dry) cleaning processes have recently been the subject of mechanistic studies, especially for removal of SiO_2 surface layers using HF [56–60]. Removal of organics by oxidation and volatilization with ultraviolet-enhanced ozone treatment (UV/O_3) has been demonstrated and investigated in considerable detail [57, 61, 62], and the removal of metal impurities from surfaces by UV/Cl_2 treatment has been reported [63]. Several new liquid cleaning reagent systems are under investigation, including NH_4F as an alternative [64] to aqueous HF, and choline as a replacement or enhancement for the standard RCA wet cleaning sequence [65, 66]. Finally, plasma-based cleaning techniques, readily usable for etching, offer an important alternative for surface cleaning. Considerable process development efforts have already gone in this direction, particularly in concert with the evolution of commercial integrated processing systems; recently, more fundamental research on mechanistic issues has begun [67–69].

An experimental research system such as that depicted in Figure 10 makes it possible to determine the consequences of surface cleaning processes, *without* exposure of the surface to reactive species (e.g., oxygen, hydrocarbons in air) between process and postprocess analysis. Results obtained for such *in situ* XPS studies [58, 70] are shown in **Figure 11,** which compares surface conditions after HF dip to those for a subsequent UV/O_3 treatment, both carried out in an inert ambient cleaning

station (glove box). Both Si(2p) and O(1s) core-level spectra demonstrate that oxygen is absent after HF dip (to <0.01 monolayers), while, as expected, the UV/O_3 treatment grows a thin SiO_2 layer. As seen from the F(1s) spectrum, the HF dip leaves a small amount of F in the surface region detected by XPS (~15–20 Å penetration depth), which has been identified as subsurface F [56, 58]. Upon UV/O_3 treatment, this fluorine is incorporated into the growing SiO_2 film in the form of oxyfluoride moieties [58].

It is very important to recognize that, in general, surface cleaning processes *add reactive species* while removing others. For HF dip cleaning, SiO_2 is effectively removed, but subsurface F is left, together with a passivating layer of hydrogen [56, 59] which completely covers the surface, ~1.0 mℓ in Si–H (monohydride) form plus ~0.5 *mℓ in* $Si–H_2$ (dihydride) form. UV/O_3 cleaning removes hydrocarbons but leaves an SiO_2 layer together with oxyfluoride species formed from prior HF treatment. The residual species left from surface "cleaning" processes play a crucial role in three areas: 1) the affinity for the surface to getter reactive impurities, even in ultraclean, integrated processing systems; 2) the suitability of the surface for the specific process step which follows the surface clean; and 3) the properties of structures formed by subsequent processes. As an example of 3), incorporation of fluorine into an MOS oxide has been shown to increase the reliability of these structures against degradation due to radiation and hot-electron effects [58, 71, 72]. Examples of 2) are the focus of a later discussion of low-temperature UHV/CVD epitaxial growth and integrated processing of thermal gate oxide structures.

The passivation properties of the wet-HF- and UV/O_3-treated surfaces have been investigated in some detail and are of great importance for subsequent processes. For HF dip cleaning, the hydrogen layer on the surface is thermally stable until desorption of the $Si–H_2$ species near 400–450°C and then the Si–H species near 550°C, and this layer greatly retards oxidation of the Si surface in air [73–76]; this behavior plays a critical role in preparing the surface for low-temperature UHV/CVD epitaxial growth [75]. However, the hydrogen passivation does not prevent adsorption of hydrocarbons, which fragment and form Si–C defect centers upon annealing sufficient to cause H desorption [77]. The UV/O_3 treatment produces an SiO_2 passivation layer more resistant to hydrocarbon adsorption; this oxide passivation layer is crucial in integrated processing of thermal MOS structures because it functions as a barrier to Si surface etching and roughening during high-temperature treatments under oxygen-deficient conditions [70].

Given the need to control a variety of reactive impurities (oxygen, carbon, metals, etc.) as well as particles, we can expect a *sequence* of surface cleaning steps which should be carried out under ultraclean environmental conditions as part of an integrated processing strategy. The need to tailor the resulting passivation species on the surface for specific subsequent processes further complicates the problem and suggests that we should consider the challenge more that of *surface condition engineering*. Much fundamental research is needed to develop the highly controlled and chemically sophisticated surface conditioning processes which are needed.

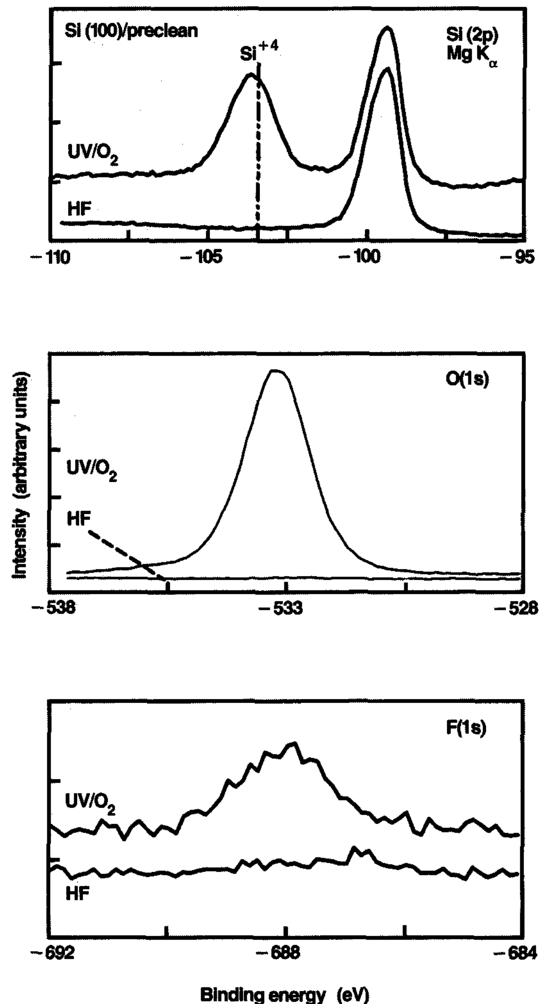


Figure 11

Surface conditions following HF dip and UV/O_3 cleaning. XPS core-level spectra for Si, O, and F after dipping into HF and subsequent *in situ* UV/O_3 cleaning, obtained using the integrated processing system in Figure 10. Surface treatments were carried out under ultraclean conditions (1 atmosphere inert ambient), and the wafers were then transferred in UHV to the XPS analysis chamber. Parts (a) and (b) from [70]; part (c) from [58]; reproduced with permission.

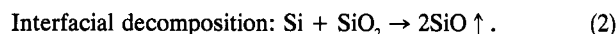
Chemistry of the silicon–oxygen system

Although such thermal processes as semiconductor growth and thermal oxidation appear straightforward, the *processes* which accomplish them sufficiently well to provide high-quality material involve more subtle chemical interactions of the silicon–oxygen system, particularly in the sense of competing reactions, as discussed above in connection with Figure 9. For deposition and especially epitaxy, the key issue is to remove oxygen from the starting surface and then to incorporate as little oxygen as possible into the growing film. For oxidation, the goal is to grow SiO_2 with a minimum of bulk and interfacial defect structures and further to maintain these characteristics under subsequent thermal and electrical stressing.

Let us summarize here the fundamental reactions of the silicon–oxygen system which are pertinent to the discussion which follows. At sufficiently high temperatures, O_2 or H_2O impingement on the Si surface induces the etching reaction, which removes Si via volatile SiO formation:

$$\text{Etching: } Si + O_2 \rightarrow 2SiO\uparrow . \qquad (1)$$

Oxygen already present in the form of SiO_2 can also be removed at high temperature by the interfacial reaction between the underlying Si or Si deposited onto the SiO_2, again through formation of volatile SiO:

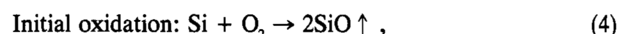


$$\text{Interfacial decomposition: } Si + SiO_2 \rightarrow 2SiO\uparrow . \qquad (2)$$

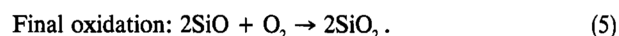
The overall reaction for thermal oxidation of Si to grow high-quality SiO_2 is as follows:

$$\text{Oxidation: } Si + O_2 \rightarrow SiO_2 . \qquad (3)$$

The early stages of oxidation involve two chemical transformations, initial oxidation to SiO and then final oxidation of SiO to SiO_2:

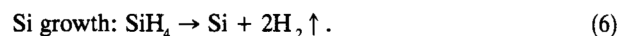


$$\text{Initial oxidation: } Si + O_2 \rightarrow 2SiO\uparrow , \qquad (4)$$



$$\text{Final oxidation: } 2SiO + O_2 \rightarrow 2SiO_2 . \qquad (5)$$

Finally, Si growth by CVD from SiH_4 is as follows:



$$\text{Si growth: } SiH_4 \rightarrow Si + 2H_2\uparrow . \qquad (6)$$

An example of the complexity which can arise within processes involving only silicon–oxygen reactions can be seen by noting that etching and initial oxidation are really the same reaction, but in the latter the SiO product is further oxidized before it can desorb. As a consequence, in the presence of low levels of O_2 or H_2O, the Si surface will be either 1) etched and roughened by the etching reaction, or 2) oxidized by final oxidation of SiO to SiO_2, depending on the relative rates of oxygen impingement and SiO formation/desorption. This situation is depicted in **Figure 12,** where the results of Smith and Ghidini [33] in the range ~900–1100°C show a kind of reaction-phase boundary, determined by the kinetics of SiO desorption, which separates temperature–pressure regimes dominated by oxidation vs. etching of the Si surface.

Low-temperature CVD epitaxy

Epitaxial growth at low temperatures (<800°C) is probably the most demanding semiconductor process with respect to control of reactive impurities, both at the starting surface (determined by the pre-epitaxial cleaning process and reaction initiation) and at the steady-state growth surface (determined by cleanliness conditions during growth). Major advances have occurred in the last few years in the quality of low-temperature CVD epitaxial growth which are a *direct* result of using ultraclean growth conditions, both at low pressure (by UHV/CVD) and at atmospheric pressure. For UHV/CVD epitaxy [34, 75, 78, 81] using SiH_4 precursor for deposition [reaction (6) above] at temperatures of 550°C [78] and below, improvements have been demonstrated not only in material characterization studies but also in the performance of a variety of electrical test structures, culminating in the fabrication of bipolar transistors which doubled the world speed record for both npn [82] and pnp [83] devices.

Recently *selective* epitaxial growth of Si [84–86] and SiGe alloys [87] has been extended to low growth temperatures (~500–600°C) using chlorosilane precursors. The ultraclean steady-state growth conditions required for low-temperature epitaxy have been achieved in these cases either by use of ultrapure reactant and reactor conditions at atmospheric pressure [84] or by exploiting rapid thermal CVD at low pressures [85–87], typically with a high-temperature *in situ* prebake to obtain initial surface cleanliness. Alternatively, selective growth in a hot-wall UHV/CVD reactor has also been reported [81]. Further work is required to demonstrate high electrical quality and device advances based on low-temperature selective epitaxy at the levels already achieved for blanket UHV/CVD epitaxy.

Although a variety of reactive impurities are deleterious to the quality of epitaxially grown material (oxygen, carbon, metals, etc.), the natural propensity of semiconductors to form oxides represents the primary problem, since even minor levels of oxidation will destroy epitaxial alignment at *all* surface sites, not just at a low density of defect sites. The conventional approach to epitaxial growth is to maintain growth temperatures sufficiently high that oxygen is always volatilized as SiO. This is accomplished prior to growth by the interfacial decomposition reaction (2), in which some of the surface Si is consumed to remove surface oxide contamination [88]. This process requires high temperatures, ~900°C for SiO_2 films of reasonably high electrical quality (e.g., thermally grown or CVD), or ~750°C for less well-defined SiO_2 (e.g., the native oxide formed at room temperature);

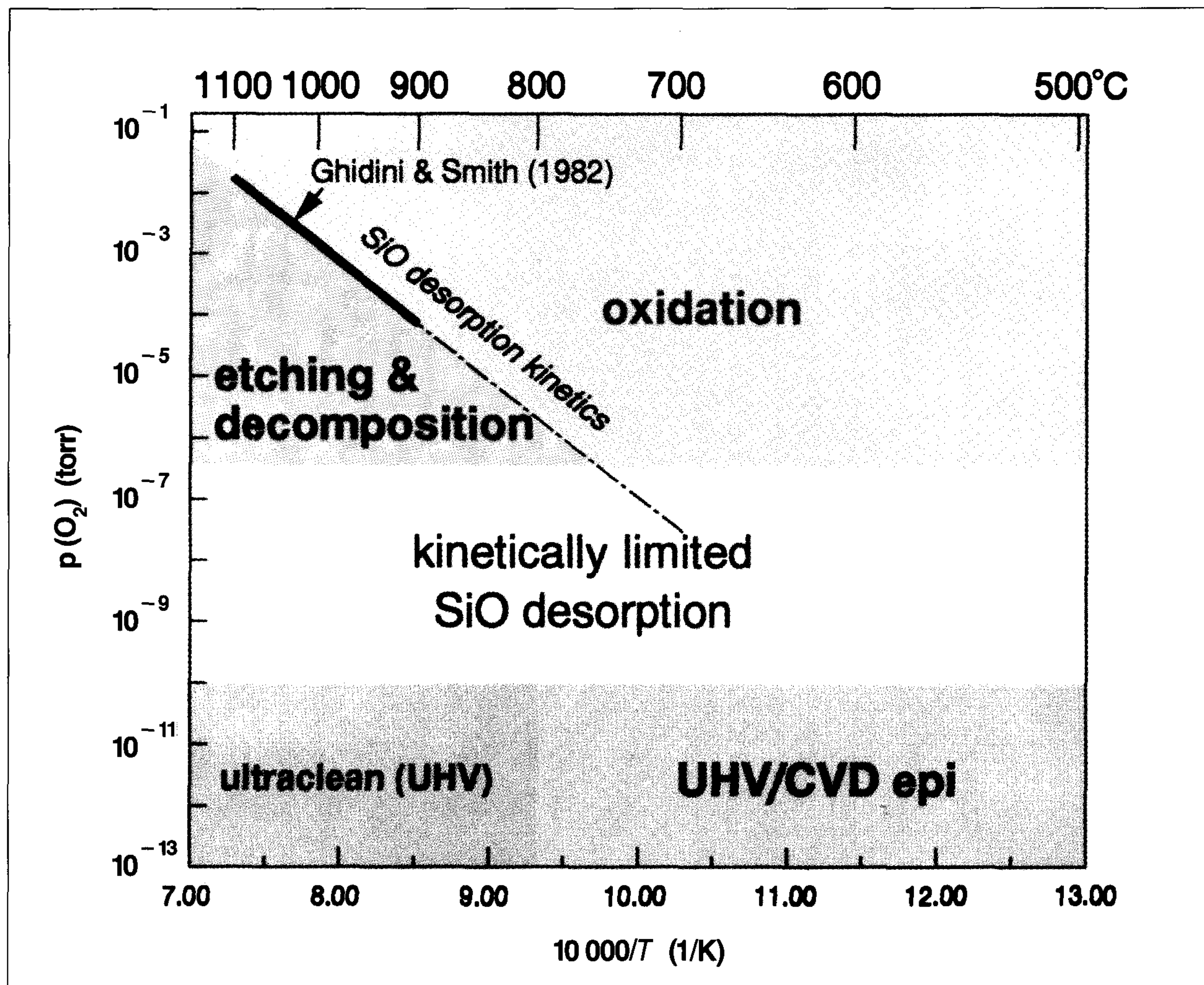


Figure 12

Fundamental chemical reactions of the silicon–oxygen system. Phase diagram for oxygen etching, decomposition, and oxidation reactions as a function of O_2 partial pressure and temperature. The phase boundary separates etching and decomposition reactions from oxidation reactions at higher temperature, allowing a mechanism for oxide removal for high-temperature epitaxial growth. At lower temperatures, these mechanisms become kinetically limited and ineffective. In the ultraclean limit (i.e., ultrahigh vacuum conditions), oxygen arrival and incorporation rates are sufficiently low to permit growth of high-quality epitaxial Si at low temperatures.

the impinging Si reactant at the initial stage of deposition also helps SiO_2 removal by "Si beam cleaning," in which the same interfacial decomposition reaction (2) occurs between the surface of a thin SiO_2 layer and the deposited Si, rather than at the buried Si/SiO_2 interface.

Once the initial oxide layer has been removed and steady-state epitaxial growth begins, the surface is maintained oxygen-free by the etching reaction (1), which ensures that low concentrations of impinging O_2 or H_2O form volatile products, rather than leading to oxygen incorporation in the growing Si film; this occurs in the Si surface etching regime indicated in Figure 12. If oxygen impingement rates exceed the rate of SiO product evolution from etching and decomposition reactions, net oxidation of the Si surface occurs and destroys epitaxial quality. The activation energy for SiO desorption is $\Delta \sim$ 3.8 eV [33], and the behavior for H_2O impurities [89] is similar to that for O_2 [33].

At lower temperatures (e.g., ≤800°C), the distinction between oxidation and etching/decomposition regimes becomes blurred by increasingly slow kinetics for SiO desorption (see Figure 12); for example, although the kinetic balance may favor etching, the rate of SiO desorption may be smaller than the impingement rate of Si reactant, causing oxygen incorporation into the film.

Standard Si epitaxy thus employs beneficial competing reactions of surface etching and decomposition to remove deleterious oxygen species before and during growth. Successful low-temperature epitaxy therefore requires alternative mechanisms to ensure the maintenance of growth conditions which do not incorporate oxygen into the growing film, as well as the removal of surface oxygen as part of associated surface cleaning.

Low-temperature UHV/CVD epitaxy
In low-temperature UHV/CVD epitaxy, ultraclean conditions are exploited to ensure sufficiently low oxygen concentrations for high-quality epitaxial growth. By employing ultrahigh-vacuum technology in the design of the growth reactor [34, 79], O_2 and H_2O partial pressures are maintained below 10^{-9} torr (typical UHV base pressures), and a regime for low-temperature epitaxy is established as shown in Figure 12. Since the oxygen impingement rate on the growth surface is small under such conditions, very low oxygen incorporation is encountered to growth temperatures of ~450–500°C (below this, Si deposition rates are very small and hence impractical). The efficacy of the process is further enhanced with respect to oxygen-containing impurities by the use of a hot-wall batch reactor: Si deposition on the walls (and on sacrificial wafers at the ends of the wafer cassette) provides a large area for efficient oxygen gettering. Finally, since the reactive sticking coefficient of SiH_4 on Si is very low (e.g., $\sim 3 \times 10^{-5}$ at 400°C) [90] and the reactor is operated under molecular flow conditions, reactant is supplied uniformly to product wafers in the batch with negligible depletion by the reactor walls or end wafers in the cassette.

Surface cleaning prior to epitaxial growth is accomplished for low-temperature UHV/CVD epitaxy using wet HF dip cleaning; this removes all oxygen from the surface and leaves a H-covered surface, well passivated against reaction with O_2 and H_2O [73–76] so that wafers may be successfully transferred in air (over several minutes) from the HF dip station to the UHV/CVD reactor. The surface passivation resulting from HF dip provides the equivalent of an ultraclean environment by greatly suppressing reactive attack by the air. Since UHV/CVD epitaxial growth at low temperature (≤550°C) involves a steady-state coverage of hydrogen (monohydride form) whose thermal desorption kinetics represents the rate-limiting step for growth [91, 92], surface conditions during growth resemble those of the HF-dip-cleaned surface (monohydride- and dihydride-covered), and a natural transition from the precleaned/passivated surface to the steady-state growth surface can be inferred. At temperatures somewhat above 550°C, hydrogen is absent from the growth surface [91, 92] and the epitaxial quality is somewhat poorer, though notably better than would be obtained using conventional epitaxial tools and processes [75] at these temperatures.

Low-temperature selective epitaxy
Selective growth of epitaxial layers is also of great interest for a variety of applications. For example, the deposition of epitaxial Si on exposed Si areas without simultaneous deposition on SiO_2 masking regions provides one avenue toward Si-on-insulator structures. Although most chemical deposition processes display some degree of selectivity at proper temperature/pressure conditions (e.g., for SiH_4 growth [81], as in UHV/CVD epitaxy), selective Si deposition and epitaxy have been most successfully carried out using chlorosilane compounds, particularly dichlorosilane ($SiCl_2H_2$ or DCS) [84–87].

A particularly interesting case is that of selective Si epitaxial growth at 600°C using ultraclean reactant and reactor conditions *at atmospheric pressure* together with a load-lock system [84]. These results showed that epitaxial layer quality requires <2 ppb oxygen impurities in the growth chamber. They also demonstrate that it is not ultrahigh vacuum *per se* which ensures ultraclean conditions and major advances in growth; rather, *ultraclean growth conditions* (with respect to deleterious reactive impurities) are the crucial factor in achieving high-quality epitaxial growth at low temperature.

Incorporation during growth: In situ *doping and SiGe alloys*
Dopant profiles are conventionally fabricated either by diffusion or by ion implantation with subsequent annealing to activate the implanted dopants. In both cases the resulting dopant profiles are determined by diffusion and are not sufficiently sharp to produce leading-edge high-performance devices. Therefore, the *in situ* doping capability of low-temperature epitaxial growth techniques provides substantial advantage. Boron incorporation in UHV/CVD at 550°C growth temperature has been achieved to $\geq 1 \times 10^{20}$ B/cm^3 active p-type dopant [78]; furthermore, these p-dopant profiles can be highly abrupt, varying over several orders of magnitude over <10 nm and enabling the fabrication of bipolar basewidths ≤50 nm. More recently, n-type doping (phosphorus) has been utilized in UHV/CVD bases ~ 45 nm in width (1×10^{19}/cm^3) for high-speed pnp transistors [93], although the tendency for surface poisoning of the growth reaction by phosphorus limits the design flexibility available for n-doped UHV/CVD epi (cf. that for p-doped material).

Recent bipolar device advances [82, 83] have highlighted the leverage of epitaxial alloy materials—specifically SiGe. Since Ge is isoelectronic with Si and can be incorporated from GeH_4, heterojunction structures can be realized which exploit bandgap engineering extensively. An

example is given in **Figure 13**, which depicts the depth profile of dopants in the npn bipolar structure as well as the Ge content in the 45-nm-thick SiGe epitaxial alloy base region; because of the ultrathin, abrupt base region and the exploitation of SiGe heterojunction bandgap engineering, this device achieved a 75-GHz f_T speed (unity current-gain cutoff frequency) twice that of the previous published record. These materials and processing advances, together with their demonstration in strategic device structures, establish reasonable credibility for manufacturing applications of heterojunction devices, ultraclean processing, and perhaps integrated processing.

Role of integrated processing

As explained above, ultraclean processing is a crucial prerequisite for low-temperature epitaxy and advanced homojunction and heterojunction device structures. The success of low-temperature epitaxy may also depend on aspects of integrated processing. The use of a wafer load-lock chamber provides an ambient buffer stage for impurity gases between the ultraclean environment of the growth chamber and the surrounding room (clean room or otherwise). After loading wafers into the load-lock, pumpdown to at least high-vacuum conditions ($\leq 10^{-6}$ torr) guarantees that minimal oxygen and other reactive impurities are introduced into the reactor with the wafers. Load-locking represents one of the earliest applications of multichamber processing and sets the stage for the more complex multichamber integrated processing systems now available for manufacturing. Whether vapor or liquid precleaning processes are used, manufacturability will likely require their integration with the UHV/CVD process reactor, either as part of a vacuum cluster tool or within a mini-environment.

The fabrication of multilayers of n- and p-type epitaxial Si and SiGe material using low-temperature epitaxy may require more sophisticated schemes of integrated processing. While some research has included the *in situ* deposition of epitaxial multilayer structures (multiprocessing, e.g., MBE-grown bipolar devices [94, 95], superlattices [96], or limited-reaction processing [36, 97, 98]), these have not yet been expanded to include multichamber CVD-based deposition of multilayers, where very specific issues of dopant and alloy concentration profiles play a critical role in determining device performance. Indeed, loading effects from different dopant precursors (e.g., long-time constants for one dopant type to desorb from walls before introducing another dopant type) may well dictate when multiprocessing must be abandoned in favor of full multichamber integrated vacuum processing to achieve very high levels of activated doping in abrupt profiles. If used in manufacturing, low-temperature epitaxial growth would constitute one of the crucial processes for advanced devices, so it is natural to

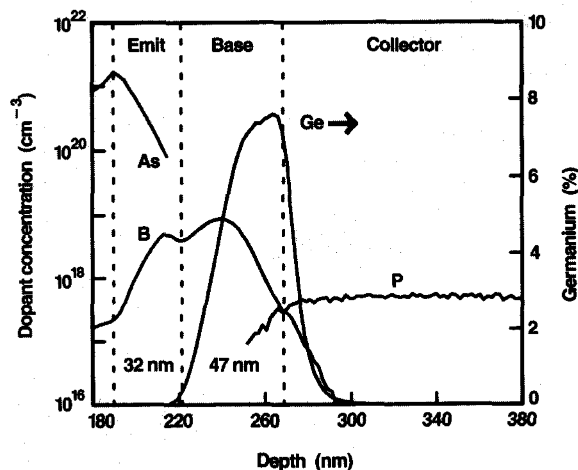


Figure 13

Advanced doping profile for high-performance bipolar devices. SIMS profile for 75-GHz f_T heterojunction npn bipolar transistor with 45-nm SiGe base region. From [82], reproduced with permission; © 1990 IEEE.

expect that these would be included in an advanced approach to integrated processing.

• *Thermal processing of dielectric structures*

The extremely high dielectric quality available from the thermal oxidation of Si(100) surfaces is often cited as the key property in the success of the Si-based microelectronics technology, because the bulk and interface properties of thermally grown SiO_2 on Si(100) determine many of the figures of merit for MOSFET and CMOS structures [99]. With the scaling of devices to smaller dimension (oxide thicknesses → 5–10 nm) and ever-higher levels of integration on a chip, defect densities resulting from gate oxidation represent a primary determinant of yield, manufacturability, and cost with which the potential performance of the devices can be harnessed. Yield and defect density goals for the foreseeable future—for particles if not also reactive impurities—have driven clean-room technology to its limits and provide substantial motivation for adopting ultraclean and integrated processing approaches to gate-oxide fabrication. It is therefore important to explore an ultraclean, integrated processing version of today's conventional gate dielectric processes in order to obtain an early evaluation of the effectiveness and chemical subtleties which might be involved in integrated processing for manufacturing.

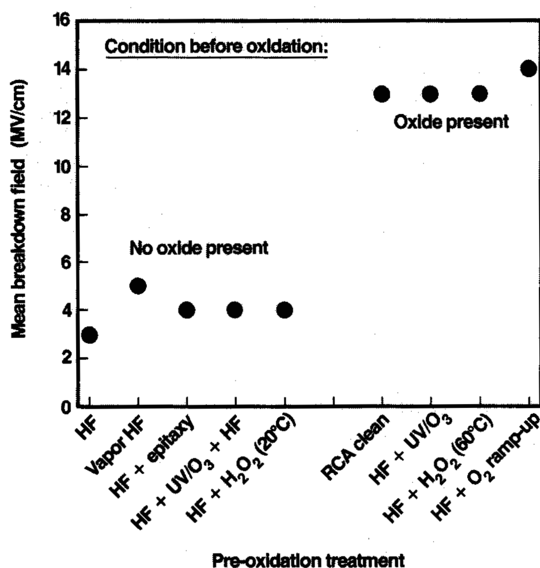


Figure 14

Oxide quality vs. final surface treatment in MOS structures. Mean breakdown field for MOS capacitors [Al gate, 12 nm SiO_2 on Si(100)] fabricated by ultraclean, integrated thermal oxide processing as a function of final surface treatment before oxidation.

Integrated surface preclean and ultraclean thermal oxidation

Ultraclean, integrated processing of MOS structures has been the subject of recent research aimed at understanding and correlating the pre-oxidation cleaning chemistry with the resulting oxide quality [70, 100]. By exploiting an advanced UHV-based custom multichamber system for integrated processing [51, 101], device-quality MOS structures have been fabricated, demonstrating for the first time the feasibility of evolving batch hot-wall reactor processes to an ultraclean, integrated processing system. However, this exercise also demonstrated that the advanced chemical control accessible with such an approach opens the door to subtle but critical process choices, and that these must be understood and mastered in order to reap the expected manufacturability advantages of multichamber process tooling.

Indications of this chemical complexity can be seen in **Figure 14,** which shows a striking and systematic dependence of dielectric breakdown quality on the atomic-scale consequences of the pre-oxidation surface treatment [70, 100]. Here RCA-cleaned Si(100) wafers (3.25-in.-diameter, p-type, 2 Ω-cm) were introduced into the inert-ambient glove-box environment for final surface treatment, transferred through a UHV load-lock and wafer transport system to a quartz cassette in a UHV-based hot-wall reactor, ramped up in temperature in 1 atm Ar ambient to 850°C, then oxidized in 1 atm O_2 for 2 h, producing ~12 nm SiO_2. Al-gate MOS capacitors were fabricated after oxidation by evaporation through a shadow mask, in some cases within the integrated processing system but usually in a separate system (for convenience).

The results in Figure 14 display two striking features. First, high dielectric strength is obtained for a variety of final surface treatments, including the RCA clean (the control), or by wet HF dip followed by an oxidizing treatment (UV/O_3 or hot H_2O_2 dip). Good breakdown behavior also results from a final HF dip combined with temperature ramp-up in O_2 rather than Ar. These breakdown characteristics are an important indication that ultraclean, integrated processing is capable of providing device-grade MOS structures. It is crucial to note that the final surface treatments which yield high dielectric breakdown strength all regrow a *thin protective oxide layer* (as shown in Figure 11 for UV/O_3) after an HF dip.

Second, a variety of final surface treatments prior to oxidation which leave essentially no protective oxide layer (as indicated in Figure 11 for HF dip) produce MOS structures with *poor* (low) breakdown strength. Such treatments in Figure 14 included wet HF dip, vapor HF clean, *in situ* low-temperature UHV/CVD Si epitaxy (carried out in the same reactor at low pressures prior to oxidation), an $HF/UV/O_3/HF$ sequence, and an HF dip followed by a room-temperature H_2O_2 dip. It is striking, and perhaps surprising, that achieving high dielectric quality through an ultraclean, integrated MOS process requires the presence of a thin oxide layer on the Si surface prior to thermal oxidation, while an oxide-free surface leads systematically to structures with poor dielectric strength.

The crucial role of oxide passivation is a consequence of the chemical nature of the silicon–oxygen system as accessible within an ultraclean, integrated processing environment [70, 100, 102]. HF cleaning processes remove essentially all oxide on the monolayer scale and passivate the surface with chemisorbed hydrogen. Upon heating to ~550°C, this hydrogen is thermally desorbed, exposing the bare Si surface [102]. During temperature ramp-up of the wafers in the ultraclean (UHV-based) oxidation reactor, O_2 and/or H_2O impurities in the atmospheric-pressure Ar are <1 ppm, but of course not zero. At sufficiently low oxygen concentrations, whatever O_2 or H_2O species *are* present induce surface etching of Si (1), a statistical process which is accompanied by roughening of the surface. Indeed, roughening of the Si/SiO_2 interface by initial surface cleaning and ramp-up has been documented by direct structural evidence (TEM [100] and STM [70]), as well as by inference from current–voltage electrical characteristics [100]. Furthermore, roughness associated with the statistics of surface etching has been shown sufficient to

cause field enhancement at asperities in the MOS structure, leading to apparent low-field breakdown behavior like that seen in Figure 14 [100].

Systematic chemical trends correlate with the occurrence of low-field breakdown to support this picture, as indicated in **Figure 15**. In these experiments, a final HF dip cleaning was followed by ramp-up and annealing for 10 min in 1 atm Ar at various temperatures and O_2 impurity concentrations to explore the consequences of annealing under etching vs. oxidation conditions, as in Figure 12. Afterward, the wafers were cooled, ramped up in O_2, and oxidized, and MOS capacitors were fabricated. For each data point represented in Figure 15, the resulting mean breakdown field of the MOS capacitors is noted. The boundary between high ($\geq$10 MV/cm) and low ($<$10 MV/cm) breakdown fields is clear, as depicted in the figure. The *slope* of the boundary (thermal activation energy) is approximately the same as that for SiO desorption, which forms the boundary between surface etching and oxidation depicted in Figure 12, demonstrating that the breakdown characteristics follow the chemical systematics of the etching reaction (1).

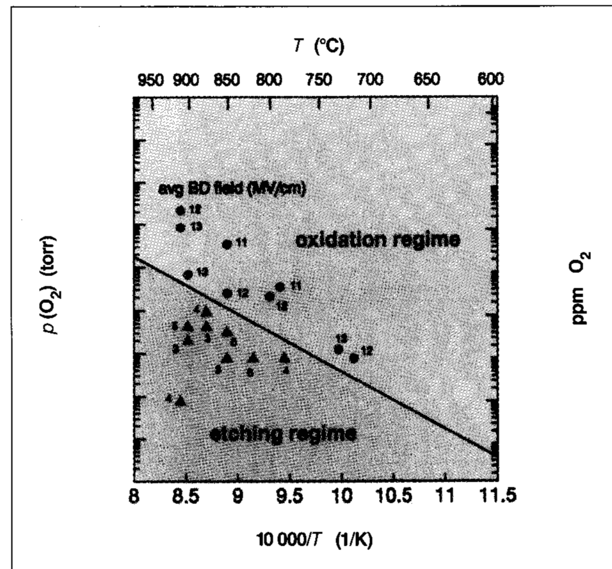


Figure 15

Chemical systematics of dielectric breakdown for integrated MOS processing. Mean breakdown fields achieved for Al-gate MOS capacitors formed by ultraclean, integrated processing. The wafers were cleaned by a final HF dip, ramped up to various temperatures (shown) in 1 atm Ar in the presence of various O_2 concentrations (shown), cooled, then ramped up in 1 atm O_2 to 850°C oxidation temperature, and oxidized.

The mechanistic understanding of these results implies specific guidelines for successful integrated processing of MOS gate-oxide structures for manufacturing, as indicated schematically in **Figure 16,** which depicts the relevant surface cleaning and oxidation processes as a function of O_2 partial pressure (H_2O would be similar) and temperature. In conventional processing [Figure 16(a)], a standard RCA precleaning is carried out in air (20% O_2). The wafers are then transported through air to a furnace-loading station, then exposed to clean-room air as well as the hot O_2 streaming out of the furnace during loading. Thus, the wafer surface is always maintained under oxidation conditions in conventional MOS processing, and no surface etching by O_2/H_2O can occur.

Ultraclean, integrated processing offers for the first time the opportunity for the reaction pathway to include the Si surface etching/roughening regime. In Figure 16(b) a conventional precleaning is followed by a final HF cleaning to remove all oxide from the surface. Since this process is carried out under 1 atm purified N_2 and followed by wafer transfer in UHV, the wafers reach the oxidation reactor without having grown a native oxide. If temperature ramp-up is then carried out in inert ambient, the Si surface reaches elevated temperature at low oxygen concentration, under which conditions (the etching regime) the surface is etched and roughened by any trace O_2 or H_2O present. In this scenario the benefits of integrated processing are significantly outweighed by degradation due to the newly accessible surface etching chemistry.

There are two alternatives to prevent degradation from etching and roughening during ramp-up. First, as indicated in Figure 16(c), sufficient oxygen (O_2 or H_2O) can be supplied during ramp-up to maintain the surface on the oxidation side of the phase boundary at all times; ramp-up in O_2 would be a simple embodiment, as is employed in conventional processing. Second, as shown in Figure 16(d), a thin passivating oxide layer can be grown on the wafer surface as the final step of the precleaning (e.g., by UV/O_3 after dipping in HF); this passivation layer prevents access to the Si surface by any oxygen-containing impurities which may be present during ramp-up. The integrity of the oxide passivation layer is sustained during ramp-up, provided temperatures are not so high that oxide decomposition (2) occurs. Clearly, both alternatives can be employed in an integrated process.

Once the implications of fundamental chemical reactions of the Si–O system are appreciated in the context of integrated processing, the specifics of reaction kinetics may also play an important role, as illustrated by three examples. First, the degree of electrical degradation due to roughening depends on the time history of temperature and oxygen concentration experienced by the wafer: The etching/roughening process should be most deleterious for higher partial pressures close to the phase boundary, but further work is necessary to determine quantitatively the statistical relationship of etching rate to asperity formation and consequent electrical degradation. Second, use of

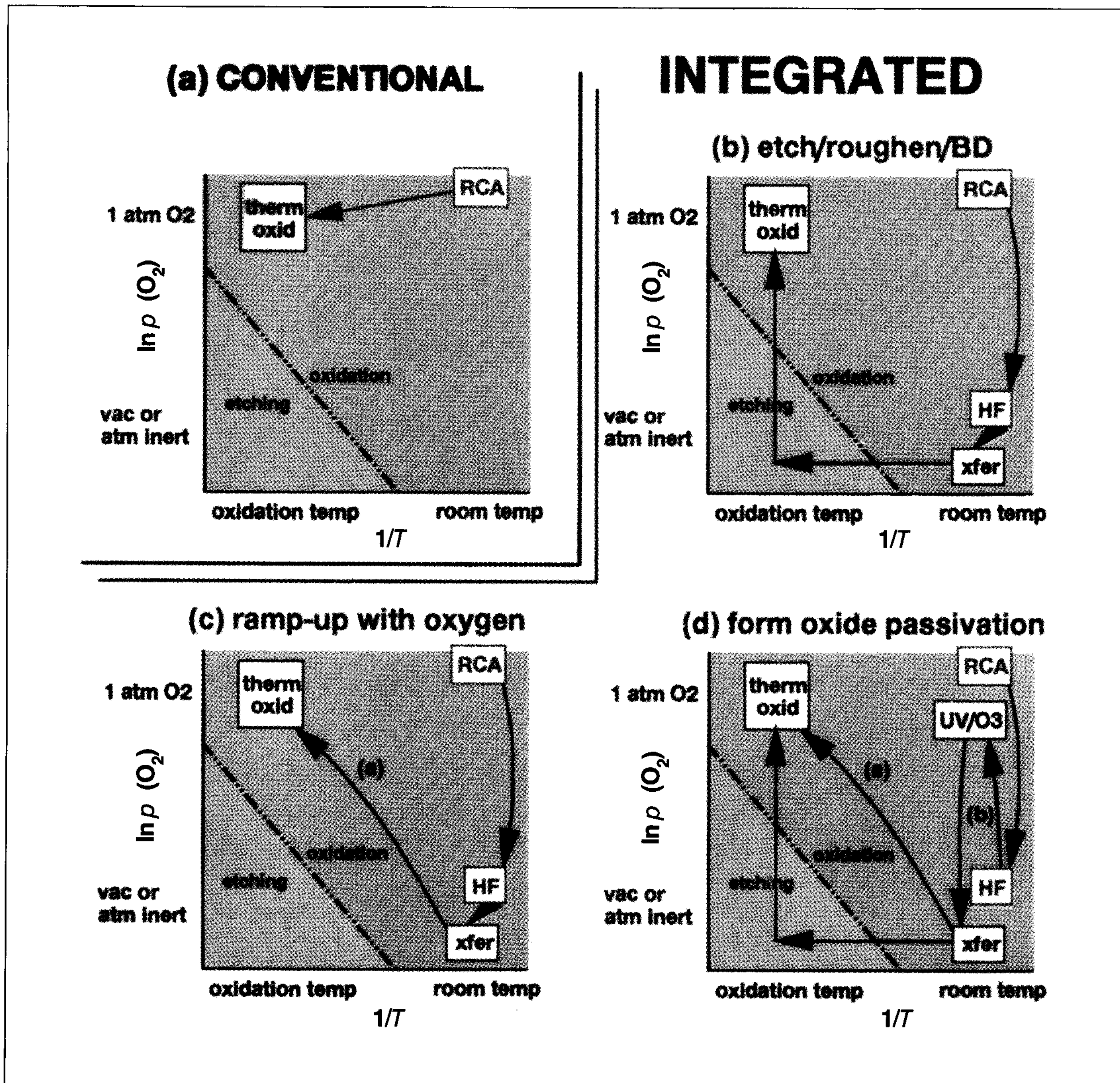


Figure 16

Guidelines for integrated MOS gate oxide processing. (a) In conventional processing, the wafer surface is always maintained under oxidation rather than etching conditions. (b) In integrated processing, the final HF-cleaned surface can be maintained oxide-free during transfer and temperature ramp-up in the oxidation reactor, thereby experiencing degradation due to etching and roughening by trace oxygen in the reactor. (c) The etching regime can be avoided by supplying sufficient oxygen during ramp-up (or by ramping up in pure O_2). (d) The etching regime can also be avoided by growing a thin passivating oxide film (e.g., by UV/O_3) as the final surface-cleaning step, thereby preventing access of trace oxygen to the Si surface during ramp-up. Portions of this figure from [70], reproduced with permission.

rapid thermal processing for ramp-up before oxidation offers the possibility of minimizing the time spent in the etching regime, an advantage compared to more conventional batch hot-wall reactor use. Third, the passivation effectiveness of an intentionally grown surface oxide depends on its stability at high temperature, i.e., the kinetics of its interfacial decomposition (2); thicker oxide layers of higher quality [e.g., thermal (cf. native oxide)]

withstand high-temperature annealing in low oxygen concentrations best, particularly if defects capable of initiating the reaction are few [88, 103, 104].

The MOSFET gate dielectric fabrication sequence of interest to future manufacturing clearly would certainly include an integrated polysilicon deposition step after the dielectric is grown. The above studies have in fact been extended to include low-pressure CVD polysilicon deposition, carried out in the hot-wall reactor following atmospheric-pressure oxidation. Preliminary results show chemical systematics similar to those of the Al gate measurements, further confirming the underlying mechanisms. Previous studies [35] have shown defect density and reliability advantages from multiprocessing of polysilicon gate MOS capacitors which combined rapid thermal oxidation, annealing, and polysilicon deposition.

In summary, these results indicate that ultraclean, integrated processing can be utilized to obtain device-quality structures within the context of integrated processing and associated tools which promise substantial defect density reduction. They also provide guidelines for practicing the integrated process sequence successfully, avoiding pitfalls which are inaccessible (and therefore essentially unknown) in conventional processing. It is important to appreciate that fundamental chemistry of the Si–O system can play critical but *different* roles in different processes: SiO formation and volatilization is destructive to integrated thermal oxide processing because the associated roughening is deleterious to MOS structures, while the same process is highly beneficial in removing residual oxide during epitaxial growth. Thus, the potential benefits of ultraclean, integrated processing can only be realized when the *intrinsic chemistry and its specificity to the desired process* are understood and controlled.

Postoxidation annealing

In conventional gate oxide processing, the thermal oxidation step is often followed by a postoxidation annealing (POA) step in inert ambient (N_2 or Ar) in order to reduce fixed charge in the oxide. The POA is typically carried out in the oxidation furnace, thus constituting an integrated process within a single reactor (i.e., multiprocessing). As with integrated thermal oxide processing described above, POA in an advanced, ultraclean tool environment opens up new dimensions of the chemistry of the Si–O system which must be understood and controlled.

By simulating ultraclean POA through annealing in an ultraclean ambient (either UHV or purified inert gas at 1 atm), morphological aspects of the oxide interfacial decomposition reaction (2) have been revealed [105]: Microvoids form in the oxide and grow laterally at high temperature (≥900°C), with Si surface self-diffusion driving reaction at the void periphery. The size distribution of oxide voids demonstrates that the decomposition process is initiated at existing defect sites in the Si/SiO_2 structure (e.g., metal impurities [104, 106]).

With annealing at lower temperatures (≥750°C), electrical manifestations of the interfacial decomposition reaction are observed [88, 105] in dielectric breakdown [107] and hole trapping [108] behavior. While oxygen-deficient annealing causes electrical activation of existing, electrically inactive defect structures, low concentrations of oxygen in an otherwise oxygen-free ambient inhibit the electrical activation of defects. As shown schematically in **Figure 17**, this suggests that the electrical activation of the defect is determined by competition between local transformations whose chemical systematics resemble interfacial oxide decomposition (2) and SiO reoxidation (5), while at higher temperatures the decomposition reaction leads to the formation of physical voids in the oxide.

These results provide a fairly comprehensive picture of the microchemical behavior of an important class of defects in thermal SiO_2/Si structures. Perhaps the most convincing evidence of this microchemistry is provided in **Figure 18**, which is very similar in character to the dielectric breakdown phase diagram in Figure 15 for etching vs. oxidation of the Si surface. Figure 18 shows the results of POA in UHV with low partial pressures of O_2 present at various annealing temperatures. For sufficiently high O_2 partial pressures (higher for higher temperature), the Al-gate MOS capacitors subsequently formed showed no low-field breakdown, while less O_2 during POA led to very significant low-field breakdown events. The slope of the phase boundary separating the two regimes matches well the activation energy for SiO desorption, as in the case of the etching vs. oxidation phase boundary for pre-oxidation annealing in Figure 15. This quantitative behavior demonstrates that the electrical activation of defects during POA follows a defect microchemistry dominated by the competition between interfacial oxide decomposition to form SiO-like species and the final oxidation of SiO-like species to electrically inactive SiO_2 material.

These POA results have important implications for ultraclean, integrated processing. In conventional processing the POA reactor normally contains oxygen impurities at least in the ppm range; as indicated by the equivalent impurity concentrations on the right-hand scale of Figure 18, these levels are usually sufficient to guarantee that existing defects will not be activated electrically by the POA. However, in an ultraclean POA ambient the electrical activation can certainly occur, particularly if the POA reactor would be part of a load-locked, integrated processing system and separate from the oxidation reactor. The solution for advanced processing is to supply sufficient oxygen during POA to prevent low-field breakdown [88, 109]. The chemical behavior is highly analogous to that

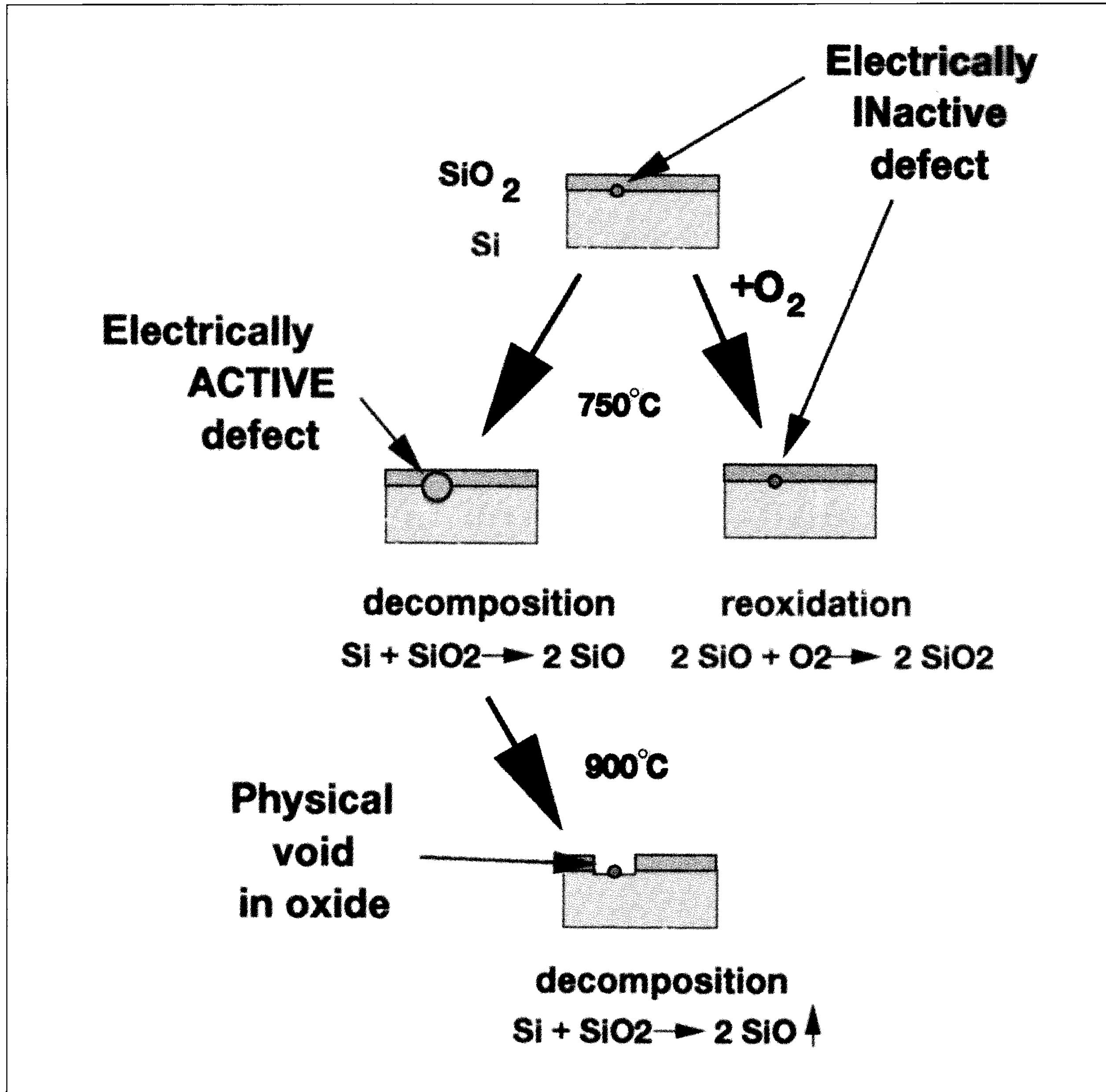


Figure 17

Defect-related chemical processes that occur during postoxidation annealing. High-temperature postoxidation annealing causes electrical activation of existing defect structures and eventually the formation and lateral growth of microvoids in the SiO_2. However, low concentrations of oxygen during annealing can prevent electrical activation as if the SiO product of interfacial oxide decomposition were being further oxidized to SiO_2.

required for advanced integrated processing for growth of the oxide, where again the process must be practiced at the oxidation/reoxidation side of the phase diagram.

Multilayer dielectric structures

Multilayer dielectric structures such as oxide/nitride/oxide (ONO) are useful in numerous applications, such as 1) incorporation of an insulating barrier (nitride) to prevent boron diffusion from polysilicon; 2) increasing the effective dielectric constant of the structure, or, alternatively, broadening the process window with respect to the physical thickness of the dielectric; or 3) reduction of defect density, since pinholes or shorts in one layer are usually covered by the other dielectric layers. Multilayer

dielectrics formed by thermal CVD [110] or oxidation processes are especially useful in high-aspect-ratio structures where a high degree of conformality over steps is essential, as in trench capacitors for high-density DRAM memory chips.

Recent results [111] on ultrathin ONO dielectrics indicate that substantial improvements can be achieved through integrated processing, specifically permitting the fabrication of ONO dielectrics under 5-nm thickness with good dielectric properties and low defect density. A common ONO fabrication sequence involves thermal oxidation, then CVD nitride deposition, and finally reoxidation of the top region of the nitride. Here it was found that a CVD oxide layer deposited *in situ* just before the CVD nitride enhanced the ability of the nitride to withstand reoxidation, i.e., to prevent further oxidation of the Si substrate during reoxidation of the nitride.

Although the detailed mechanisms responsible for this behavior are not currently understood, the results illustrate the variation in properties which can be obtained by exploiting integrated processing. Clearly, the surface upon which the CVD nitride deposition is initiated plays an important role in determining the chemical and/or physical properties of the nitride film. One could imagine rather profound differences in the surface properties of an air-exposed thermal oxide (e.g., OH radicals) compared to a CVD oxide maintained in vacuum (e.g., surface H), which might have substantial influence on subsequent chemical processes, particularly where initial nucleation or initiation of the reaction is important. In very thin multilayer dielectric structures, there remains an important challenge to characterize the depth-dependence of composition and chemical bonding as a function of process and thermal cycling, and furthermore to identify microscopic mechanisms responsible for specific electrical properties.

Multiprocessing of dielectric structures
Integrated processing of MOS structures has also been carried out in a multiprocessing mode, employing a single rapid thermal CVD/oxidation system to perform several steps *in situ* (limited reaction processing [37]). By combining rapid thermal oxidation (1150°C at 500 torr) with polysilicon CVD, MOS capacitors with reasonable midgap interface state density and fixed oxide charge were obtained, and rapid thermal annealing after polysilicon deposition produced excellent interface characteristics (midgap interface state density ~5×10^9 cm^{-2} eV^{-1}) [37]. Multiprocessing has also been employed to fabricate MOSFET structures by *in situ* combination of selective epitaxy, rapid thermal oxidation, and CVD polysilicon [38].

Multiprocessing has also been used to fabricate multilayer dielectric structures in rapid thermal CVD systems. Rapid thermal oxidation, nitridation (by NH_3),

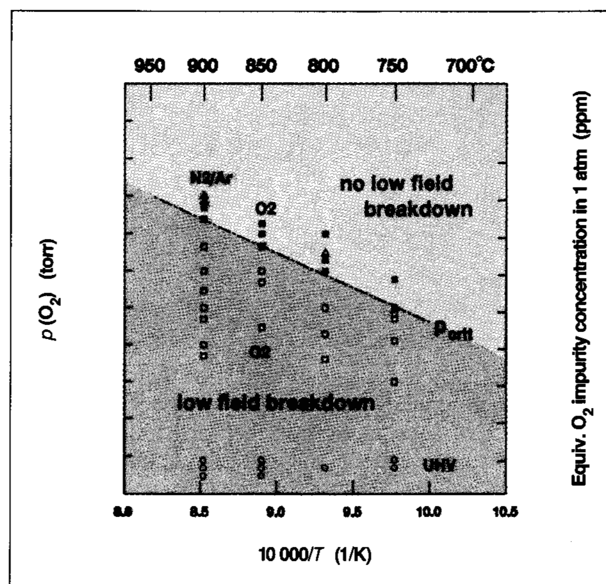


Figure 18

Chemical systematics of dielectric breakdown for postoxidation annealing. Mean breakdown fields achieved for Al-gate MOS capacitors subjected to ultraclean postoxidation annealing at various temperatures and O_2 partial pressures (in vacuum). Without sufficient O_2, low-field breakdown is observed, with a phase boundary parallel to the activation energy for SiO desorption. The equivalent O_2 impurity concentration for these O_2 pressures in a 1-atm inert ambient are shown on the right-hand scale. Portions of this figure from [109], reproduced with permission.

and reoxidation have led to improvements in hot-carrier immunity [112] and in transconductance at high normal field and at low temperature [113, 114]. ONO structures formed by rapid thermal CVD multiprocessing [40] have been shown to yield improved reliability [115].

- *Integrated plasma processing*

Plasma processing already plays an essential role in microelectronics process technology. Dry etching dominates patterning of submicron feature sizes (e.g., for MOSFET gate length definition), which in turn represent the cutting edge of the technology, and it is commonly considered more strategic and extendible than wet etching because of the better linewidth and vertical profile control and cleanliness of dry processes. Plasma processes are also in wide use for deposition, particularly for inorganic insulators (oxide, nitride) to isolate interconnections (wiring); in this case, the plasma excitation of reactant species allows deposition at lower substrate temperature than do corresponding thermal processes, thereby achieving compatibility with the limited thermal stability of interconnection metallizations and advanced device

structures (e.g., hyperabrupt boron doping profiles). Because of their importance in current manufacturing, these plasma etching and deposition applications have been the main focus for the first generation of multichamber manufacturing tools for integrated processing.

Plasma deposition of gate dielectric structures
Recent research has demonstrated that plasma-enhanced chemical vapor deposition (PECVD) can produce materials of sufficient electrical quality to serve as "active" dielectrics (e.g., MOSFET gate) or semiconductors, in addition to "passive" dielectrics used to isolate interconnection lines. These advances have resulted from several new process and tool practices, including remote plasma excitation [116, 117], downstream introduction of less stable reactants (e.g., SiH_4) [116], ultrahigh-vacuum-based reactor design [118], low-rate deposition with heavy dilution in He [32, 117, 119] and *in situ* plasma surface pretreatments [118, 119]. Applications of new PECVD processes to devices are numerous, ranging from MOS capacitors, p-i-n devices, MOSFETs [32], EPROM devices [41], and α-Si thin-film transistors [41, 120], to critical passivation dielectrics in advanced high-speed bipolar transistors [32].

These investigations have highlighted some of the central issues for ultraclean, integrated plasma processing. One is the role of surface cleaning prior to deposition, where clearly both should be carried out in an integrated processing tool. Experiments using remote PECVD with UHV-based tooling suggest that the semiconductor/dielectric interface quality can in some cases be improved when the final substrate cleaning process step is performed in the same chamber as the dielectric deposition [118]. If lithographic processing has been carried out and organic resist residues must be removed from the surface, H_2 plasma cleaning is effective, although complete carbon removal may require ultraclean process environments and likely separate plasma cleaning and reaction chambers.

Control of competing reactions is another central issue arising from integrated plasma processing research. Both direct PECVD using low deposition rate in heavy He dilution [119] and remote PECVD [118] can yield device-quality dielectrics. In the former, a He plasma pretreatment (intended as a surface preclean [119]) in fact causes slow plasma oxidation of the Si surface due to oxygen-containing impurities in the ambient, which in turn establishes interface electrical properties of high quality. Similarly, dielectric deposition by remote PECVD requires that subcutaneous oxidation of the Si occur, but not in excessive amounts [121, 122]. One might infer that interface quality is rather sensitive to the balance among plasma oxidation of the substrate, plasma-induced damage to the substrate, and deposition of the overlayer, so that advanced levels of control and cleanliness in the process are essential.

Finally, important issues of thermal budgets and process integration have been raised. The low deposition temperatures of PECVD are a prerequisite for active dielectrics and semiconductor materials in low-cost, large-scale thin-film-transistor applications (e.g., active-matrix liquid crystal display technology). In advanced bipolar and CMOS applications, however, the early fabrication steps for active portions of the devices can be carried out at considerably higher temperatures. To date, remote PECVD dielectrics achieve quality approximately comparable to that of thermally grown dielectrics, but higher-temperature annealing steps must be included [41], and PECVD deposition of the polysilicon gate is considerably slower than LPCVD deposition. Advantages of plasma-based integrated processing for gate dielectric structures lie therefore in the realm of a lower thermal budget [shorter annealing time (cf. growth time at the same temperature [41])] or the process and/or tool simplification of an all-plasma deposition process sequence.

Plasma-enhanced CVD epitaxy
Plasma-based processes also offer an alternative approach to achieving low-temperature epitaxial growth. Single-chamber multiprocessing, involving low-dose argon-ion bombardment cleaning followed immediately by Si PECVD growth, has been used for growth of epitaxial Si at temperatures in the range 750–800°C [123–125]. More recently, ultraclean PECVD has been used to lower epitaxial growth temperatures to ~150°C in combination with a multistep sequence of *ex situ* precleaning, wafer introduction, and *in situ* hydrogen plasma cleaning [67, 126, 127]. An alternative approach to plasma-based processes for low-temperature epitaxy has been pursued using bias sputtering. Here ultraclean processing techniques have been exploited with *in situ* surface cleaning by sputtering in order to achieve high-quality epitaxial Si at temperatures as low as 250–350°C [128–130]. Nevertheless, it remains to be seen where lower epitaxial growth temperatures than those of UHV/CVD are needed.

Plasma-based etching
With patterning so central to the fabrication of three-dimensional structures, and with the trend toward dry as opposed to wet processing, dry etching [131, 132] and lithographic definition should probably be considered the backbone of microelectronics fabrication. At the same time, dry etching processes tend to be the most prevalent source of difficulty in achieving consistent process results and in transferring process recipes from one tool to another. These factors underscore the leverage associated with advancing our understanding and ability to control dry etching processes.

In spite of this complexity, there has been substantial progress in recent years in identifying the mechanisms which dominate etching characteristics, including both gas and surface chemistry and physics. For example, the formation of involatile reaction products often plays a critical role in establishing etching selectivity [133, 134], an important phenomenon for both the stability of the etch mask material and the ability to stop the etching accurately at the desired material interface. Etching reaction products and their susceptibility to chemical attack and directional ion bombardment play key roles in sidewall passivation and other mechanisms which control the vertical profiles of etched structures. Finally, because ion energies often exceed thresholds for material damage, the evaluation of process-induced defects and their electrical consequences appears prominently in research on dry etching processes [135–138].

The use of integrated processing systems in research, such as to combine dry etching processing with *in situ* surface analysis [133, 139], has been a major factor in achieving this kind of insight, particularly for the case most studied—reactive ion etching (RIE). A variety of other plasma-based etching approaches are attracting serious attention for manufacturing applications, including the use of remote plasma sources (with the plasma generated away from the wafer and transported to it), enhanced plasmas, as in magnetron ion etching or electron cyclotron resonance (ECR) etching [140], and cryoetching (low-temperature etching, in which the relative importance of chemical vs. physical factors can be changed dramatically). With the broad scope of fundamental and practical variations these different approaches encompass, advanced research in dry etching offers great promise to contribute to the evolution and refinement of advanced manufacturing processes and tools. At the same time, dry etching offers perhaps the greatest process challenge, because it is the process which most drastically couples microstructure modifications in the vertical and horizontal dimensions within the parameters of a single process; as witness, simply consider the fact that advanced DRAM manufacturing will require etching of structures with aspect ratios (ratio of vertical to horizontal dimension) of ~30–50.

• *Interconnections and contacts*

With higher-performance devices and their incorporation into increasingly dense circuits, time delays in signal propagation along interconnections are becoming one of the gating factors in circuit and system performance. This has driven efforts in both chip wiring and packaging to develop improved materials—lower-resistance metallizations and lower-capacitance insulators—and better strategies for optimizing multilevel interconnections [141]. At the same time, because the interconnections are put into place only after the investment has been made in fabricating the active devices, process yield in the manufacturing of interconnections is a crucial determinant of product cost. These considerations have helped place contacts and interconnection applications at the forefront of commercial integrated processing technology.

Research applications of integrated processing have focused primarily on the fabrication of contacts and multilayer metallurgical structures in which control of impurities (especially oxides) can have a major influence on electrical properties. The resistance of Al/Si contacts can be significantly reduced [142] if reactive impurities (particularly oxygen) are minimized by a suitable integrated processing sequence consisting of a N_2-gas-sealed cleaning and drying process, wafer transport in a N_2 ambient, and subsequent low-energy *in situ* ion-bombardment cleaning prior to Al bias sputtering [143].

High-performance circuits typically require more complex metallizations which incorporate a contact metal and a conducting diffusion barrier layer between the contacts and interconnections (e.g., to prevent Al penetration from Al-based lines to the Si device) [144–146]. The potential importance of gaseous reactive impurities in such structures is underscored by the observations that 1) many effective diffusion barrier metallurgies are metal nitrides or oxides; 2) interfacial reactions often lead to the formation of Al_2O_3 interlayers in Al-based metallizations, where the product Al_2O_3 performs the function of the diffusion barrier [147, 148]; and 3) while nitrogen or oxygen incorporation into the metallization may form an effective barrier layer and provide thermal stability and reliability of the contact, excessive amounts (especially oxide) can have a very adverse effect on the contact resistance.

Recently, studies employing UHV-clean evaporation and controlled O_2 dosing have verified the sensitivity of diffusion-barrier performance and contact resistance to the amount of oxygen incorporated into the barrier-layer structures [149]. Such experimental approaches appear very desirable for optimizing electrical properties and thermal stability as a function of reactive impurity concentrations in the process ambient, an advantage similar to that described earlier for integrated thermal processing of dielectric structures.

The contact structure most critical to performance and most sensitive to incorporated impurities is probably the emitter contact of high-speed bipolar transistors, which constitute the basis for today's highest-performance computing systems. Such contacts are typically fabricated by exposing and cleaning the surface of the epitaxial Si emitter region, then depositing on it a polysilicon contact metallization. It is clear that microscopic characteristics of the polysilicon/silicon contact [150–152], particularly interfacial oxygen impurities and the microstructure of the

interfacial region, strongly influence the performance of bipolar transistor devices by modifying the recombination and blocking of minority carriers which reach the interface [150]. Given that a specific amount of impurity and certain types of microstructural consequences are optimal for device performance, tailoring of this interface by ultraclean, integrated processing would appear to have high potential value.

Real-time process monitoring and control

Although significant reduction in particulate and reactive impurity contamination levels can be gained through ultraclean, integrated processing, an advanced and balanced strategy for processing technology requires an additional element—real-time process monitoring and control. For research this provides the opportunity to fabricate more sophisticated structures which yield new levels of performance or insight. For manufacturing and development, real-time process control promises major reductions in manufacturing cost, not only through higher yield and product reliability, but also by enabling greater tool utilization and dependability [44, 45].

The leverage of real-time process control ranges from the rather mundane and practical to highly sophisticated embodiments, all having great potential impact. Two applications are directed at short-term practical improvements which enhance *manufacturing productivity*:

- *Disaster recovery.* By sensing in real time the condition of the tool and process, it is possible to optimize how the process tool responds to serious and sometimes sudden failure. For example, if a leak should develop in the process chamber or a gas supply line, or if a sensor should drift off-calibration or fail, it is important to detect the failure and automatically shut down the tool in such a way as to minimize damage to the tool and if possible to any product wafers in it.
- *Preventive maintenance.* Real-time monitoring of the tool and process can be used to signal when conditions are drifting out of specification, at which point a decision may be made to carry out preventive maintenance. This is particularly important because information feedback cycles in microelectronics manufacturing are long: A process can drift out of spec many steps—often representing weeks of time—before product measurements detect the problem. Such failures often trigger major efforts to identify which tool or process step is at fault, to introduce a fix, and to verify its success. With complex tools and processes, it is far better to sense and respond to process/tool maintenance needs than to rely solely on a predetermined preventive maintenance schedule for a subset of possible repair problems.

While these applications can have immediate benefit in manufacturing productivity, two others promise advances in *product quality, performance, function*:

- *Process control.* By monitoring and controlling the environmental conditions experienced by the wafer, real-time control offers enhanced reproducibility of the product, such as ensuring constant pressure, temperature, or flow rates independent of the tool or its history.
- *Material and structure control.* In some sense the ultimate goal of real-time process control should be to control process conditions based on sensor inputs directly related to the material or structure on the wafer, rather than to the process environment, so that the characteristics of the product are rigorously determined and reproduced.

Research in materials and processing is increasingly benefitting from the application of *in situ* and real-time diagnostic techniques to provide insight into mechanistic issues as well to ensure a high degree of control of process conditions. Many of these techniques can be applied with sensitivity and control on the nanometer or atomic scale (e.g., ~0.1 nm sensitivity from ellipsometry). This should enable not only the fabrication of thin-film structures with high accuracy and reproducibility, but also the formation of new *kinds* of structures through what might be termed *nanoprocess engineering*. Examples of nanoprocess engineering include the growth of SiGe epitaxial layers with graded Ge concentration in depth to optimize bipolar device performance; ultrathin and/or multilayer dielectric structures tailored for high performance (e.g., low leakage with high capacitance) or high reliability (e.g., specific levels and distributions of fluorine in SiO_2 [71, 115, 153–155]); and dry etch engineering in which some conditions are optimized for most of the process (e.g., high rate and directionality) while the final etch to an interface is optimized differently (e.g., low damage).

The use of grazing-angle optical emission interferometry for flexible endpoint detection [156] illustrates aspects of the feasibility of nanoprocess etch engineering for the case of CHF_3 etching of SiO_2 over Si. By using optical emission from the plasma and detecting at near-grazing angle from the surface (75° from the normal), optical interferometry yields a more rapid variation in signal with depth than does conventional normal-incidence laser interferometry. As shown in **Figure 19**, a quarter-oscillation corresponds to 30-nm depth, and the interface is reached at maximum signal slope, permitting detection of a specific depth to ±3 nm at a predetermined height above the interface (or at the interface). This capability should enable advanced etch engineering, such as etching most of the SiO_2 etch with high directionality and rate, detection of a transition point

(e.g., at 20 nm ± 3 nm) above the interface, and switching at that point to another set of etch parameters which will minimize damage to the Si substrate, enhance selectivity, etc., while perhaps sacrificing a minor degree of directionality.

A system view of the apparatus required for effective real-time process control is shown in **Figure 20.** Given a process tool and a set of diagnostics installed on the tool, three additional elements are necessary. First, a method for automated control of tool parameters is needed to rapidly execute instructions from the real-time diagnostics subsystem. Second, a diagnostics controller must be in place to supervise the diagnostic measurements, make real-time decisions, and transfer instructions to the tool controller. Both controllers should be computer-based and flexible in software and hardware in order to adapt to a variety of specific instruments and applications. Third, a vehicle for diagnostics analysis must be included to distill diagnostic information rapidly and thereby provide specific instructions to the tool controller. Mathematical algorithms, look-up tables, and sophisticated control approaches (e.g., adaptive process control) can be effectively employed, both in developing recipes from calibration experiments to identify data-filtering algorithms and in calculating appropriate responses from real-time data during the process.

Although not all process situations allow effective real-time process *control* (e.g., high-rate etching), many processes are amenable to such control with known diagnostic techniques. And there is significant value in capturing diagnostic data itself, e.g. for preventive maintenance of tools. The increased use of diagnostic techniques and control methodologies should have a major impact on microelectronics research, development, and manufacturing, particularly where *in situ* and real-time measurements can be carried out.

Conclusions

Integrated processing has become a dominant trend for microelectronics process and tool technology in manufacturing and in development, as well as a prominent approach for associated research in materials and processing science. Despite its clear importance, many (if not most) of the key issues, from manufacturing to exploratory research, remain to be rigorously investigated. We have portrayed the field in broad scope, including in it vacuum-based multichamber processing systems and atmospheric-pressure mini-environments which will both play an important role, emphasizing ultraclean processing and real-time process diagnostics and control as crucial elements and natural trends.

In microelectronics manufacturing, as yet there has probably been insufficient experience with integrated processing to accurately gauge its cost-benefit advantage.

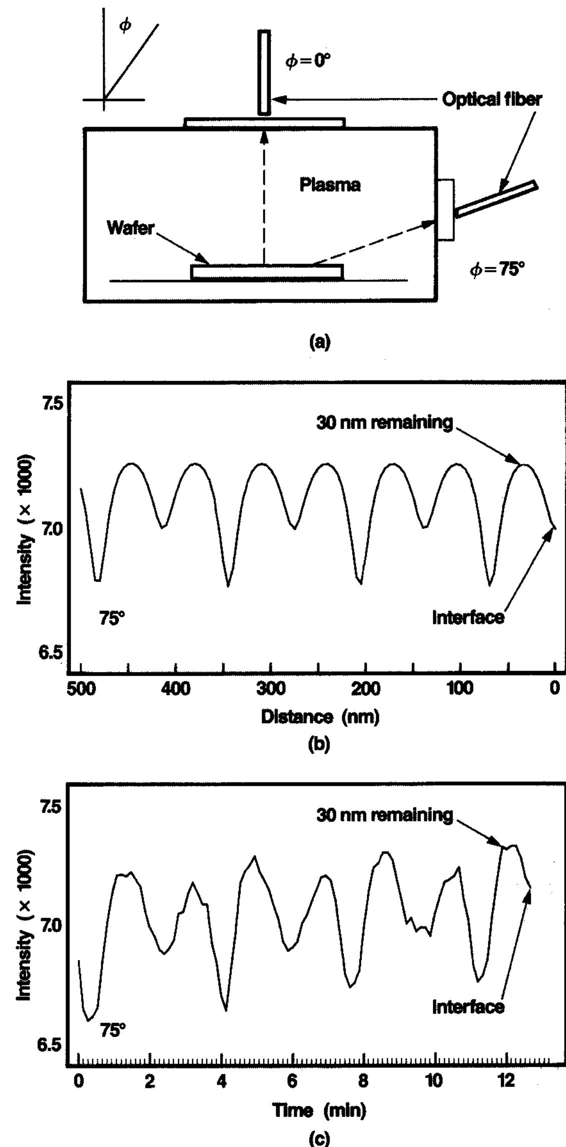


Figure 19

Flexible endpoint detection using RIE real-time process control. (a) Grazing-angle optical emission interferometry uses the plasma emission as a light source and grazing observation to enhance interferometric sensitivity. (b) Calculated and (c) experimental signals as etching proceeds to the interface. From [156], reproduced with permission.

Nevertheless, it appears to be the only credible path to the lower contamination and defect levels that will be required in the future. The trend toward ultraclean processing (and especially the reduction of reactive impurities as well as particles) should enhance process quality and

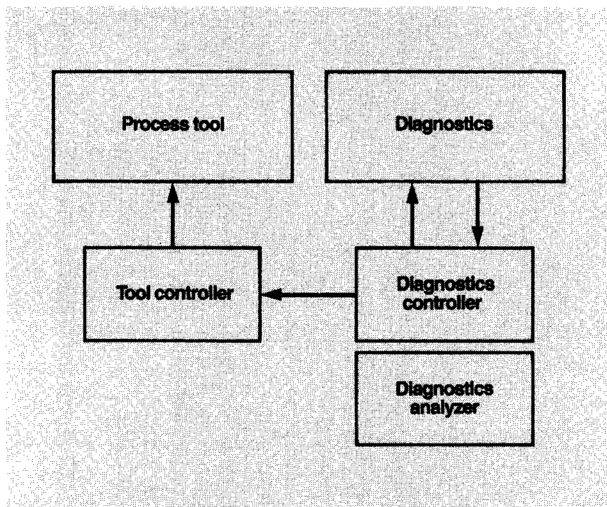


Figure 20

Methodology for real-time process control. Key elements required for effective real-time process control include an efficient tool-control system, a rapid diagnostics controller, and algorithms for digesting diagnostics information to yield in real time the parameter changes necessary to tune the tool.

reproducibility. Integrated process tooling offers potential advantages in tool flexibility, while real-time process control promises improved tool reliability.

Processing equipment (tooling) plays a central role in integrated processing. Architecture and design issues abound. Despite a justifiable and continuing emphasis on single-wafer processing, batch processing continues to offer practical attractions (e.g., cost and throughput) as well as fundamental motivations (e.g., uniformity and cleanliness of hot-wall reactors for some reagent systems), so that flexibility in tool designs seems especially valuable. Standardization of mechanical and system interfaces is expected to be pivotal if microelectronics manufacturing is to capture the advantages promised by integrated processing.

Integrated processing offers major advantages in microelectronics development as well, which span those foreseen in both manufacturing and research. Improved processes, materials, and structures can be expected from reactive impurity control in process modules and in wafer transfer chambers, as well as from real-time process diagnostics and control. With interprocess ambient control obviating the need for some cleaning and inspection steps, it should be possible for process simplification to become a reality, reversing to some extent the historical trend toward more steps.

Related research in materials and processing science has for some time emphasized the use of ultraclean environments and extensive *in situ* and real-time diagnostics, and the need for *in situ* microanalysis and fabrication of multilayer test structures has increasingly driven a focus on multichamber processing and analysis systems. Integrated processing systems for research have provided substantial insight into chemical and physical mechanisms in such areas as surface cleaning, epitaxial growth, thermal oxidation, annealing, plasma deposition and etching, thermal CVD, and multilayer metallization.

Through different pathways, integrated processing capabilities from microelectronics manufacturing and research are evolving toward a similar state, which includes the use of multichamber processing systems, ultraclean conditions, and advanced diagnostics and control. This presents an additional opportunity for research—that of prototyping integrated processing to anticipate issues resulting from relevant chemical and physical phenomena and to assess manufacturability at an early stage. One lesson has been that the highly controlled environment of integrated processing opens new reaction pathways which must be understood and controlled, as in the case of integrated MOSFET gate oxide processing. In this sense research can directly serve the needs of development and manufacturing.

Another lesson has been the importance of monitoring and controlling reactive impurity levels, a key to low-temperature epitaxy. In some cases this also means intentionally adding in a controlled fashion low concentrations of appropriate impurities, such as the intentional addition of oxygen in an integrated gate-oxidation sequence or in postoxidation annealing.

Finally, ultraclean, integrated processing and real-time process diagnostics and control promise still more exciting and open-ended directions. Greatly enhanced levels of process control should enable the development of *nanoprocess engineering*, in which multilayer microelectronic structures of semiconductor, insulator, and conductor materials can be fabricated with near-atomic (nanometer) control to achieve performance and reliability improvements. And given the sophistication which the field of microelectronics has achieved to date with a minimal level of control over reactive impurities between process steps, it is intriguing to imagine what possibilities may be realized with the advantages of the higher levels of such impurity control inherent in the integrated processing approach.

Glossary

Integrated processing: An approach in which a sequence of two or more chemical and/or physical processes is carried out while the wafer is maintained in a confined, clean, and highly controlled ambient between process steps; do not confuse with *process integration*.

Central wafer handler (CWH): Wafer transport system, enclosed in a control ambient, which is used to move

wafers between various process and load-lock chambers to accomplish integrated processing.

Multichamber (or cluster) tools: Chemical and/or physical processing system which utilizes several wafer-processing chambers (or modules) linked together by a wafer-transport system in a controlled ambient to accomplish integrated processing.

Integrated vacuum processing (IVP): Multichamber processing system in which process modules and central wafer handler are maintained under vacuum.

Mini-environments: Multichamber processing system in which process modules and central wafer handler are maintained at atmospheric pressure (preferably purified inert ambient).

Multiprocessing: Integrated processing carried out as a sequence of processes within a single process chamber.

Load-lock: Wafer transport chamber used as a vehicle for transferring wafers from room ambient to process chamber or integrated processing system, or vice versa.

Ultraclean processing: Processing carried out under cleanliness conditions which are leading-edge with respect to particulate and/or reactive impurity contamination; applies to process chambers (reactors) and to wafer-transport systems (CWH and load-locks).

Real-time process monitoring and control: Exploitation of diagnostics during process to control process parameters for reproducibility and stability.

Key clusters: Specific process sequences which are highly sensitive to defects (particles and/or reactive impurities), for which the expected advantages of integrated processing (especially ultraclean) will be most significant.

Process integration: The task of selecting and arranging individual process operations to ensure their compatibility and success in fabrication of the product, essentially independent of tool details and the means of product transfer between processes.

Fab: Manufacturing facility for fabrication of microelectronic devices.

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